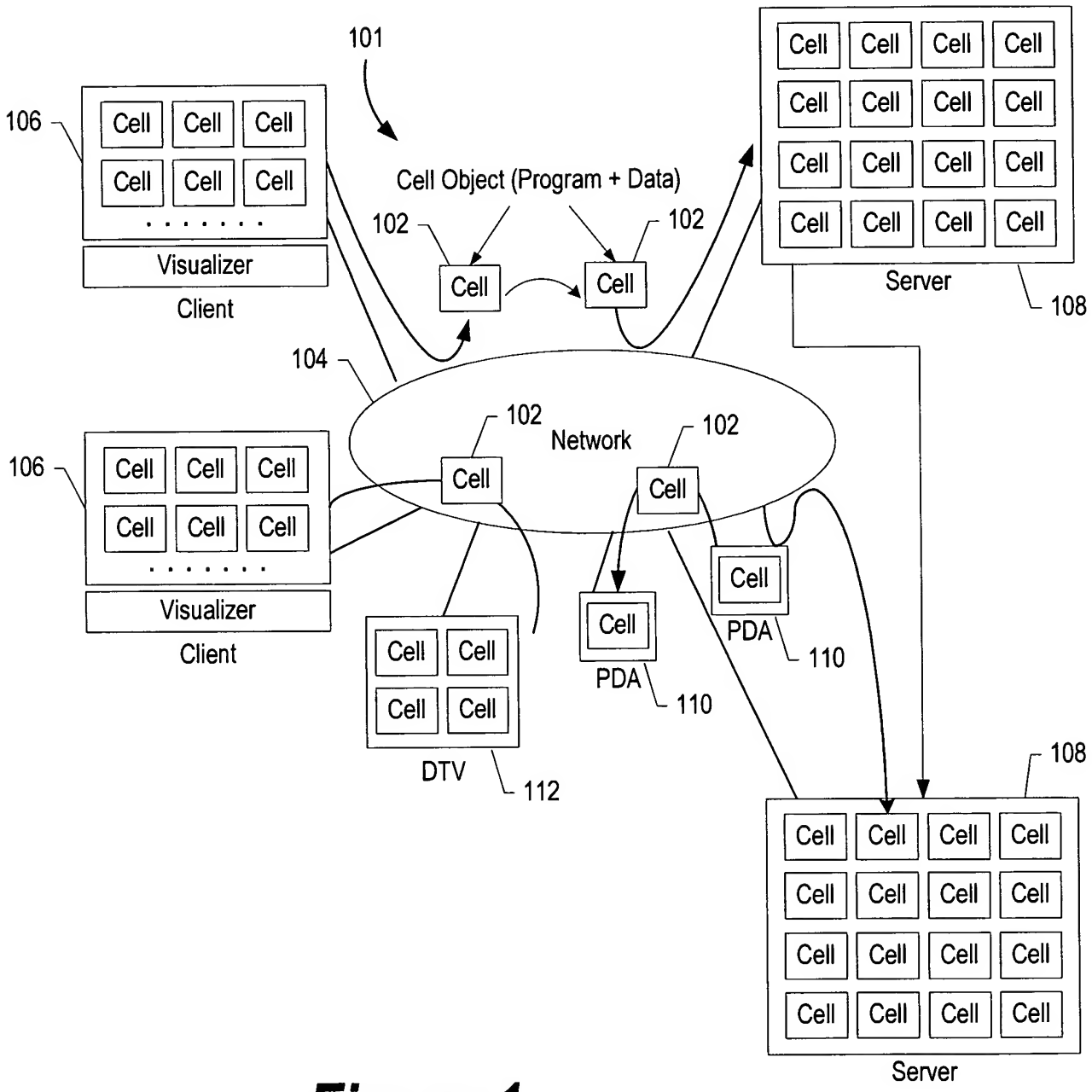
101
Cell Object (Program + Data)
102
102
Cell
Cell
106
Visualizer
Client
104
Network
Server
108
PDA
110
DTV
112

Figure 1

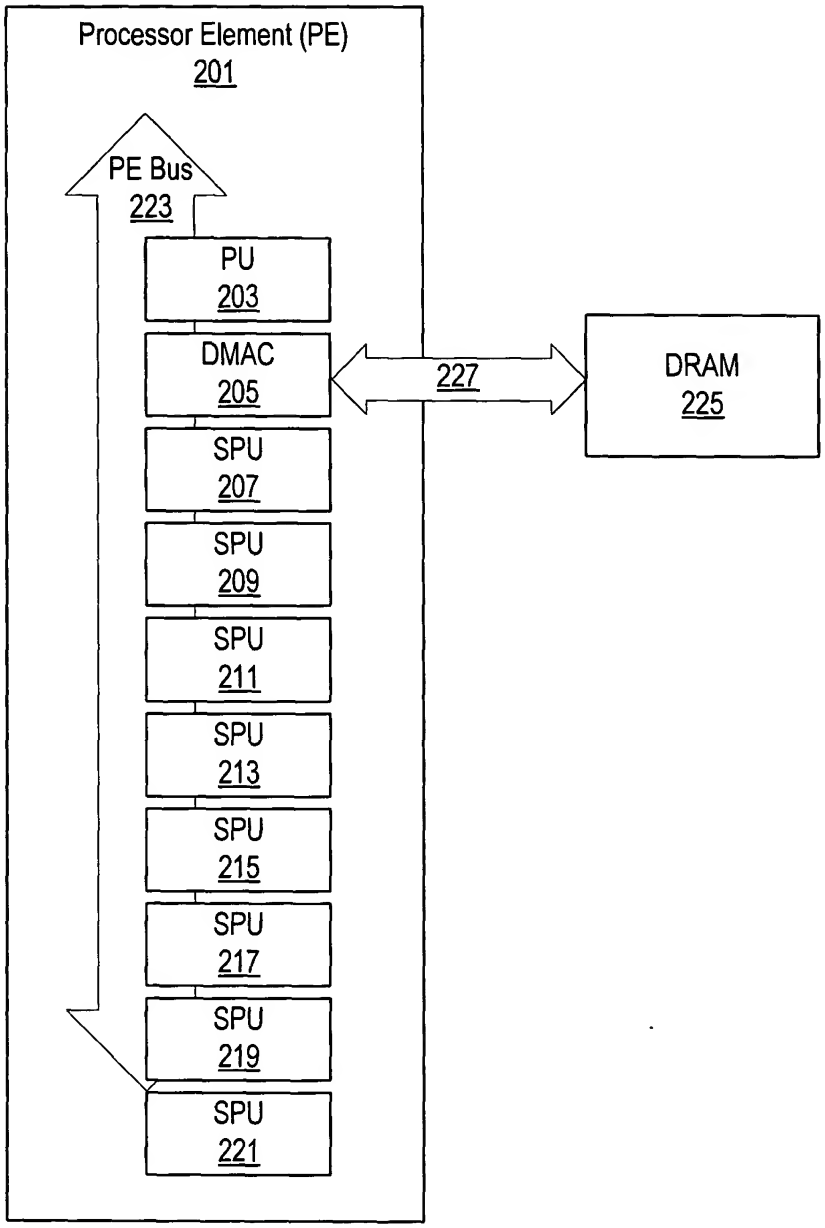
Processor Element (PE)
201
PE Bus
223
PU
203
DMAC
205
227
DRAM
225
SPU
207
SPU
209
SPU
211
SPU
213
SPU
215
SPU
217
SPU
219
SPU
221

Figure 2

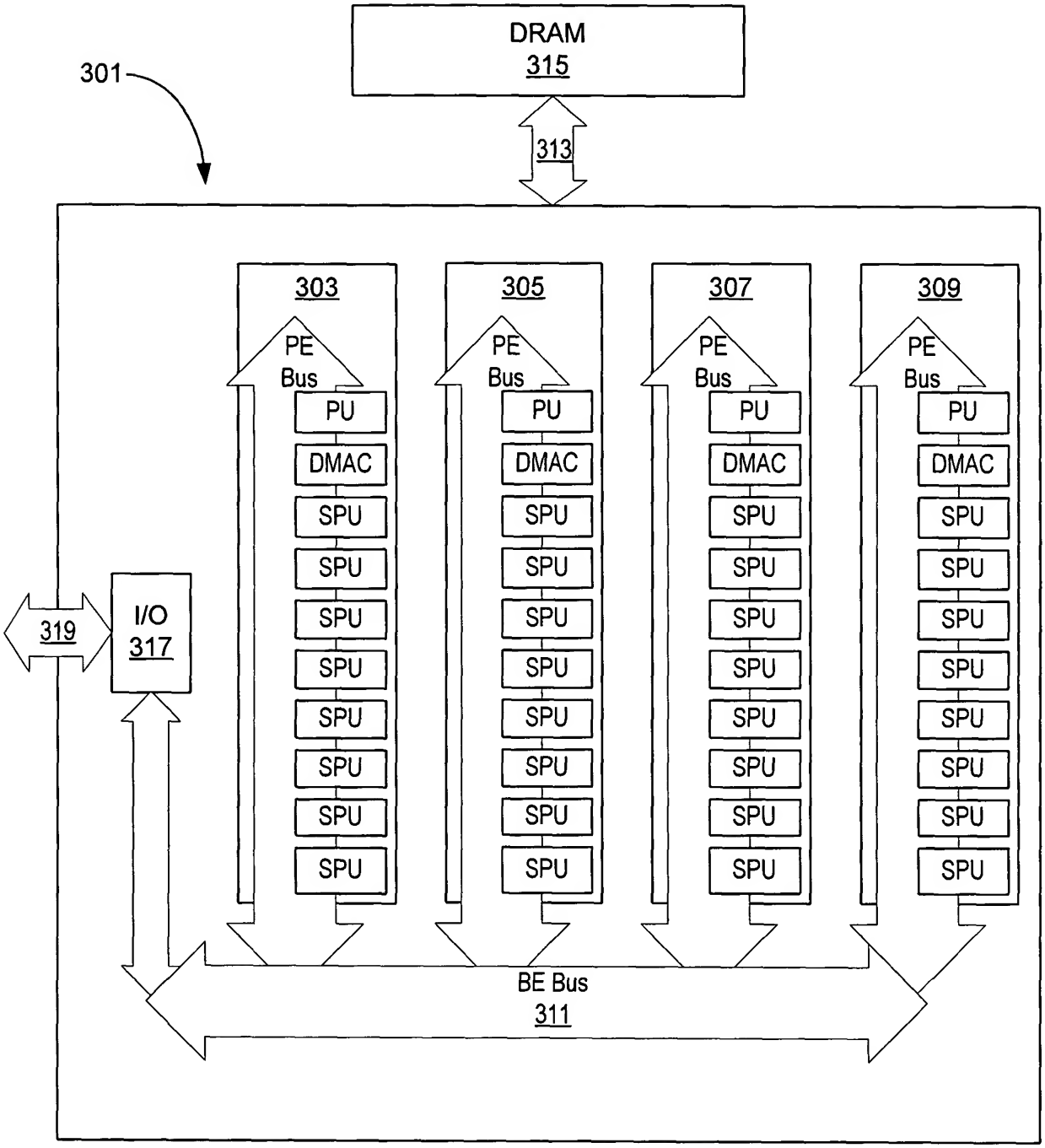
DRAM
315
301
313
303
305
307
309
PE
Bus
PU
DMAC
SPU
I/O
317
319
BE Bus
311

Figure 3

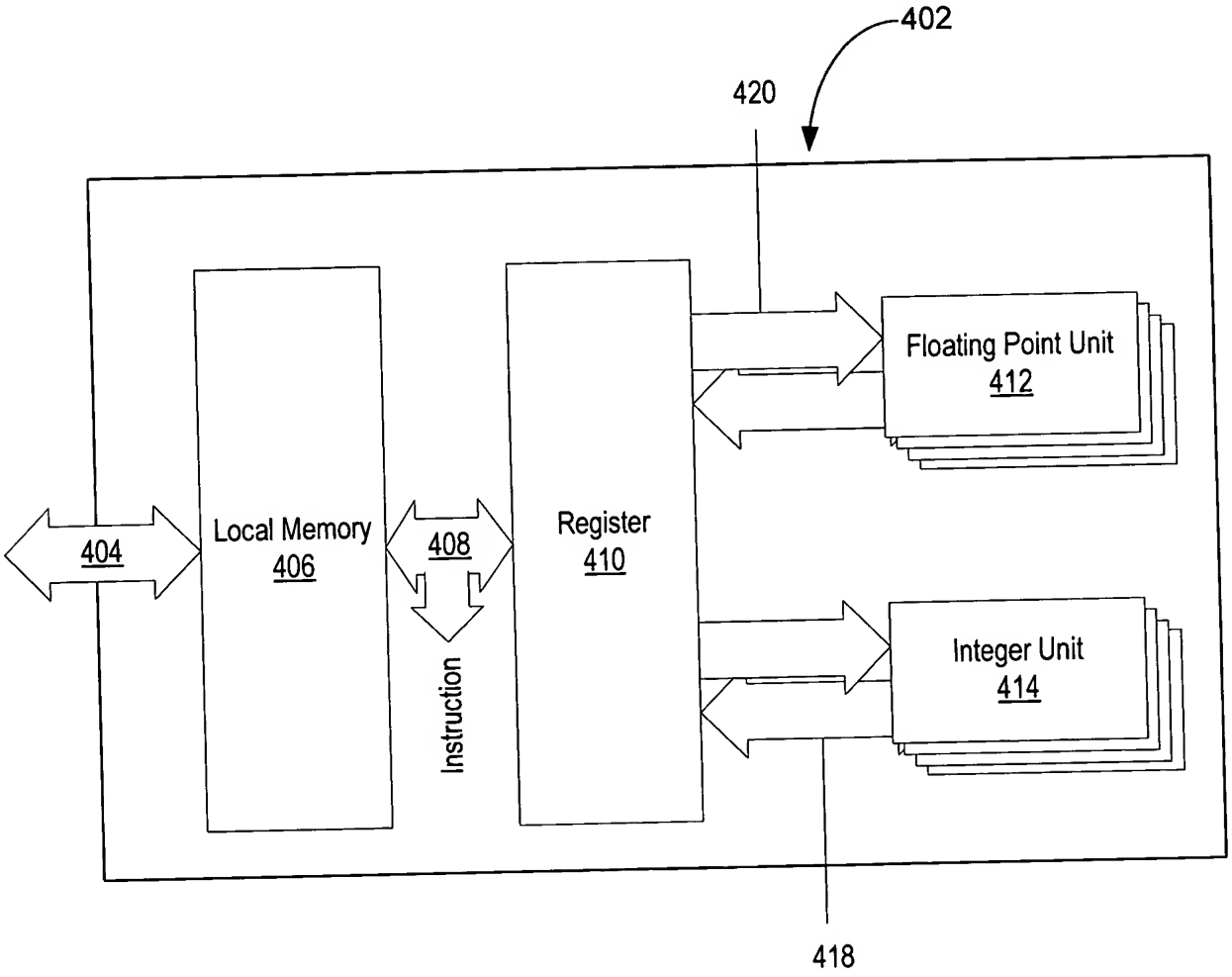
402
420
Floating Point Unit
412
Local Memory
406
404
408
Register
410
Instruction
Integer Unit
414
418

Figure 4

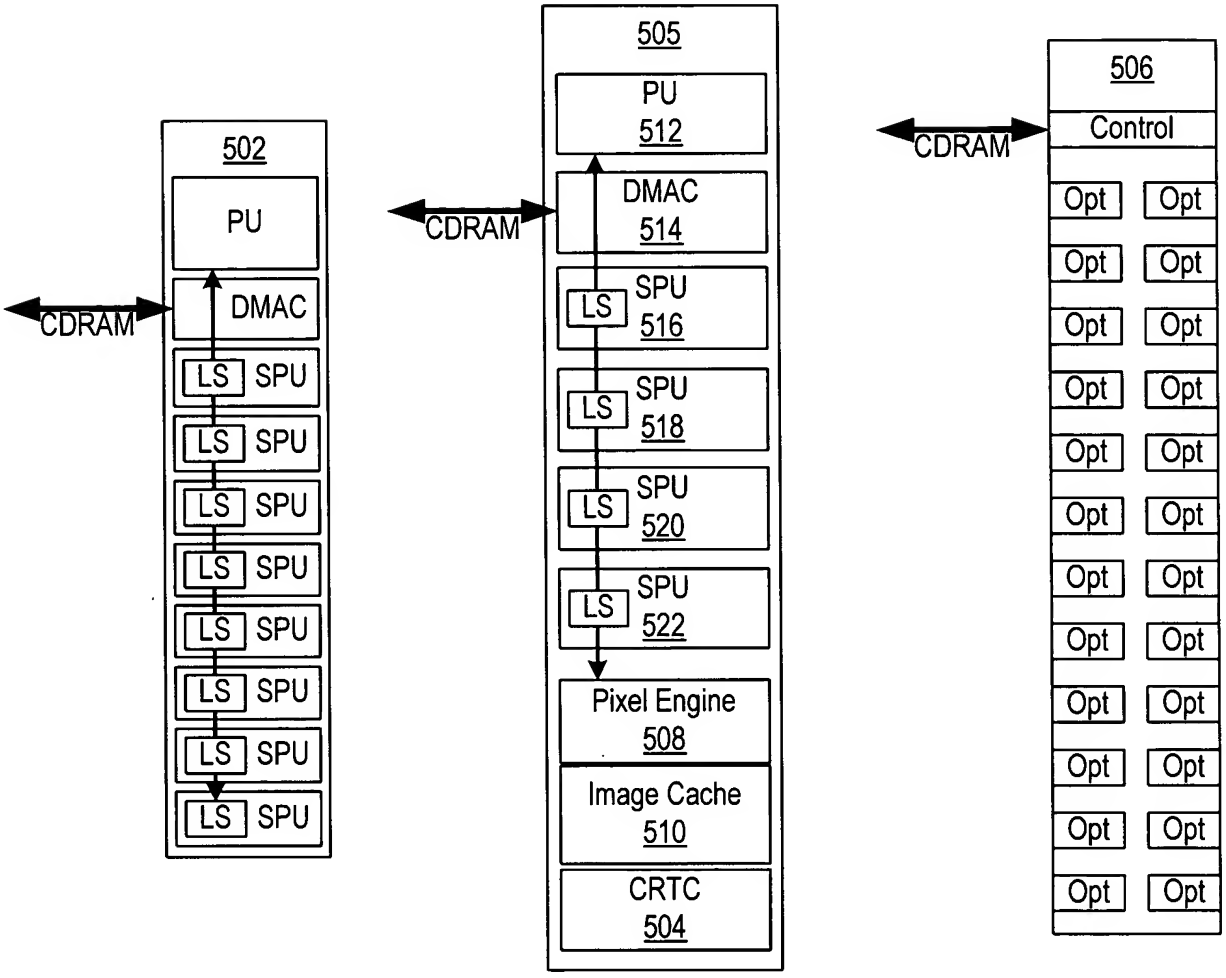
502
PU
DMAC
CDRAM
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
505
PU
512
DMAC
514
CDRAM
LS SPU
516
LS SPU
518
LS SPU
520
LS SPU
522
Pixel Engine
508
Image Cache
510
CRTC
504
506
Control
CDRAM
Opt Opt
Opt Opt
Opt Opt
Opt Opt
Opt Opt
Opt Opt
Opt Opt
Opt Opt
Opt Opt
Opt Opt
Opt Opt

Figure 5

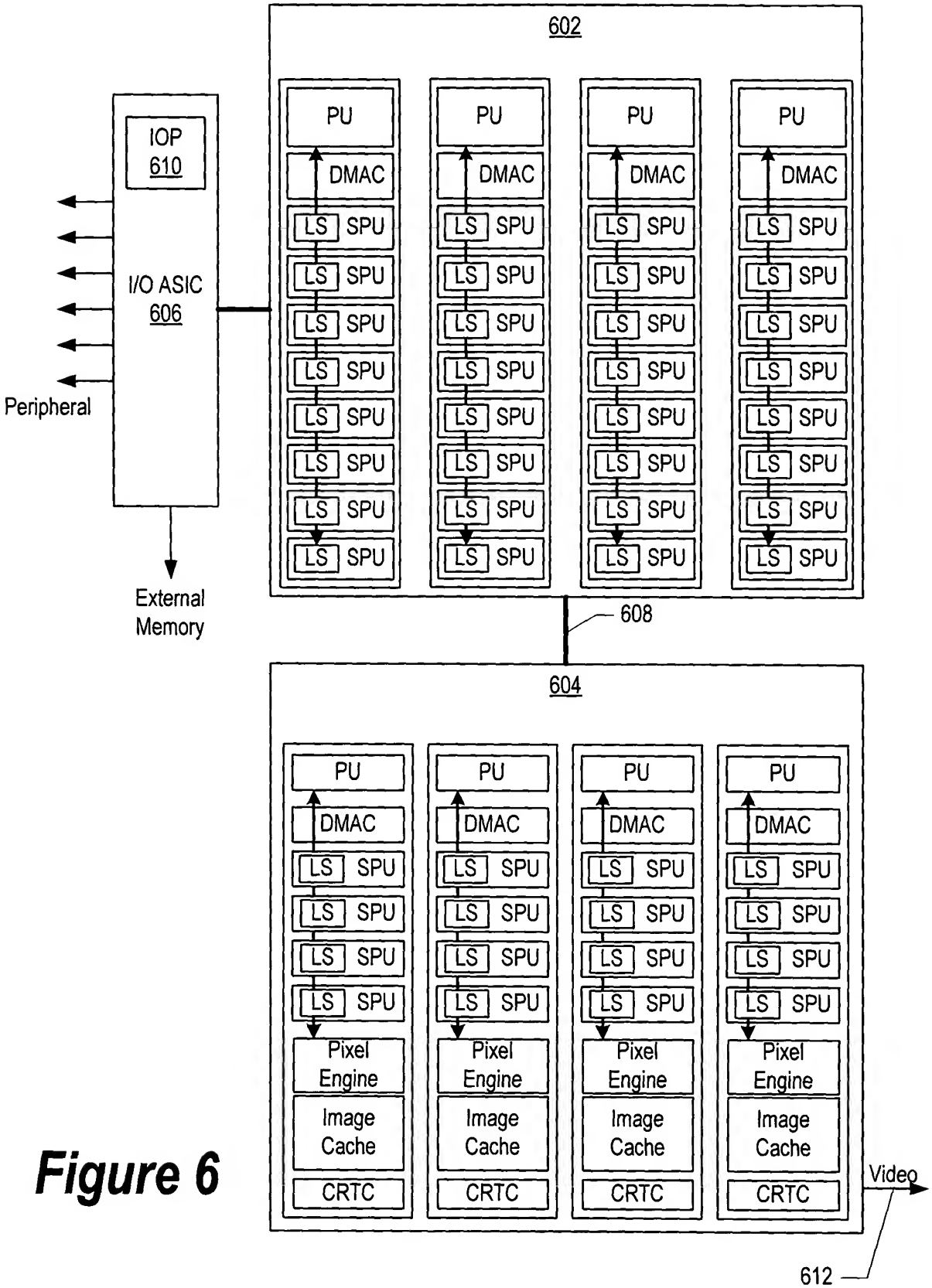
602
IOP
610
I/O ASIC
606
Peripheral
External
Memory
PU
DMAC
LS
SPU
608
604
Pixel
Engine
Image
Cache
CRTC
Video
612

Figure 6

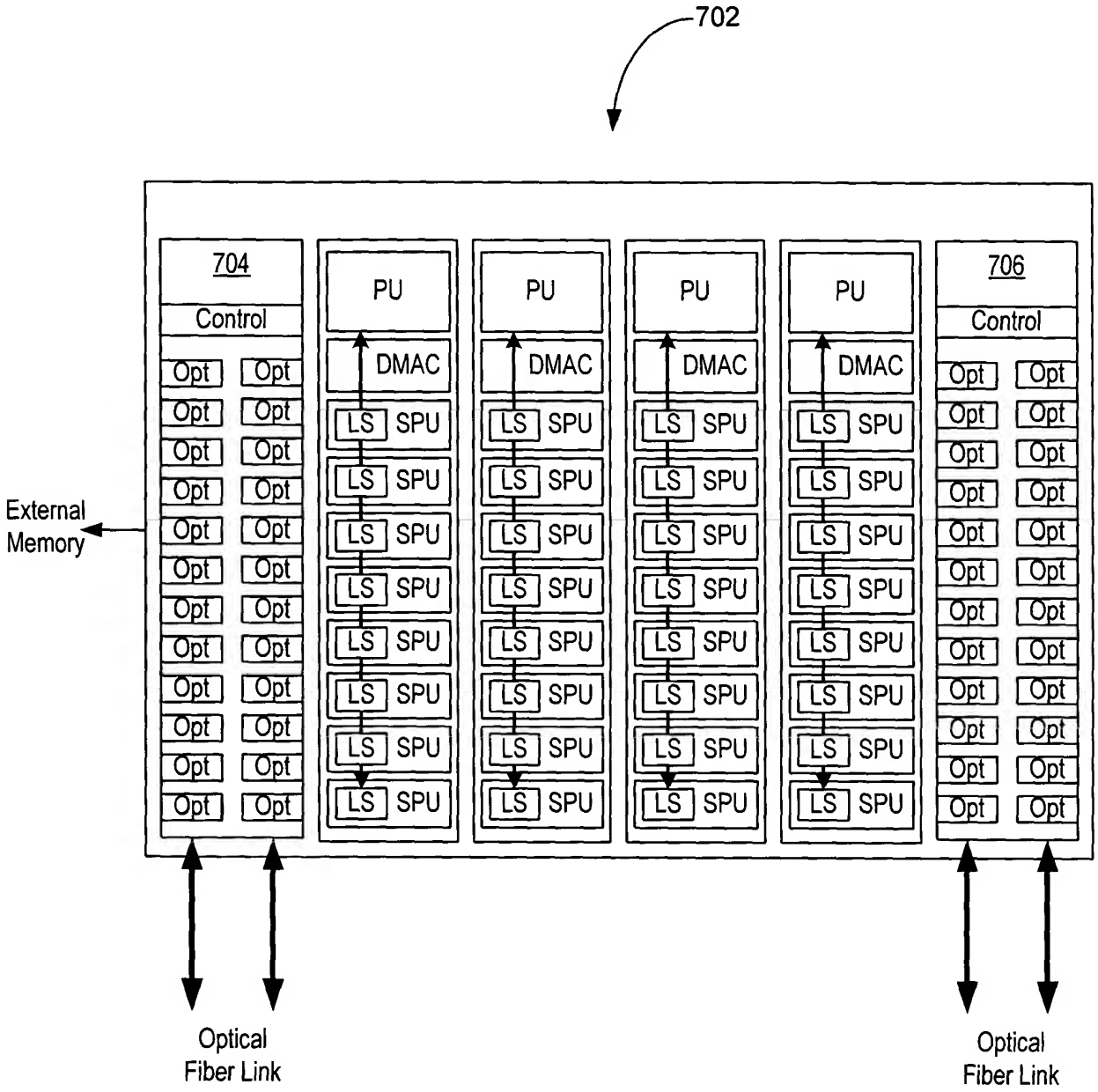
702
704
Control
Opt
706
Control
Opt
PU
DMAC
LS
SPU
External
Memory
Optical
Fiber Link
Optical
Fiber Link

Figure 7

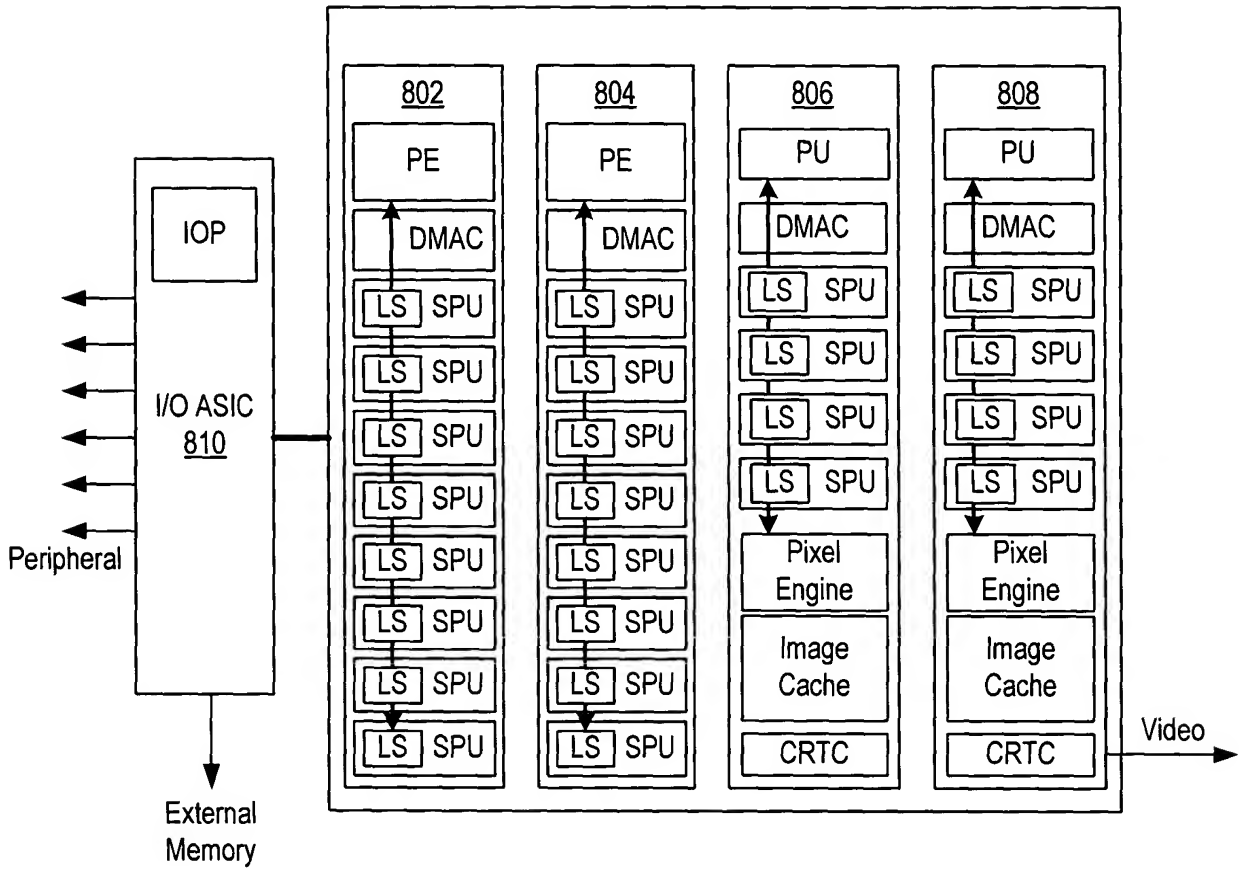
802
804
806
808
PE
PE
PU
PU
DMAC
DMAC
DMAC
DMAC
LS SPU
Pixel Engine
Image Cache
CRTC
IOP
I/O ASIC 810
Peripheral
External Memory
Video

Figure 8

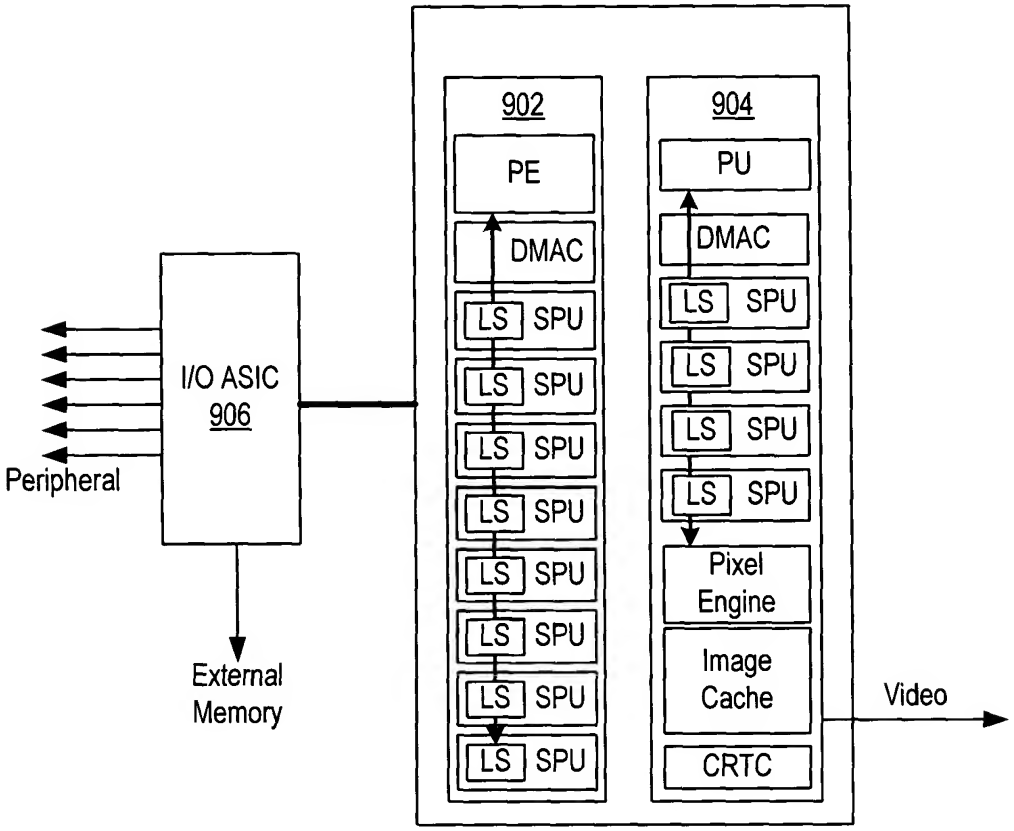
902
PE
DMAC
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
LS SPU
904
PU
DMAC
LS SPU
LS SPU
LS SPU
LS SPU
Pixel Engine
Image Cache
CRTC
Video
I/O ASIC
906
Peripheral
External Memory

Figure 9

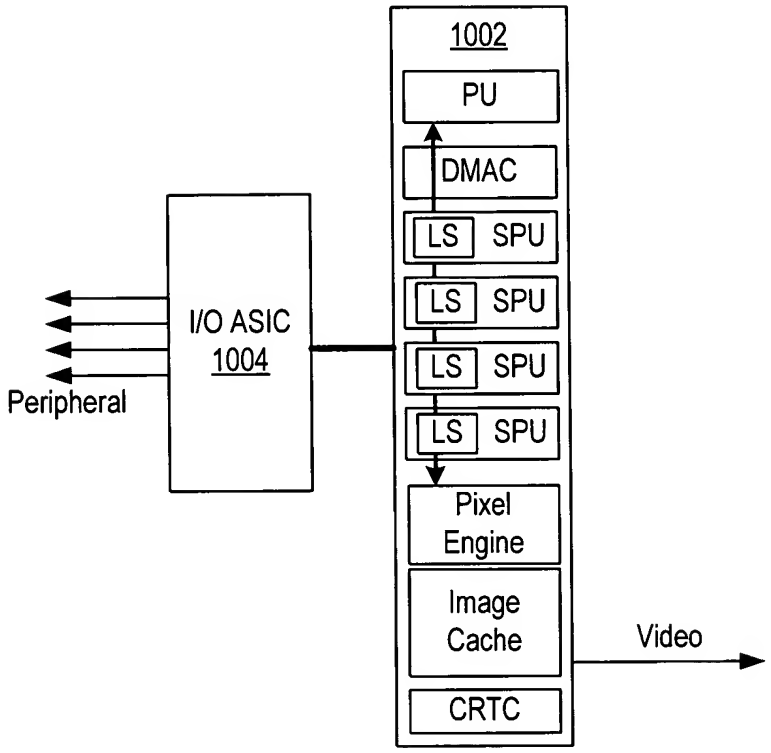
1002
PU
DMAC
LS
SPU
LS
SPU
LS
SPU
LS
SPU
Pixel Engine
Image Cache
CRTC
Video
I/O ASIC
1004
Peripheral

Figure 10

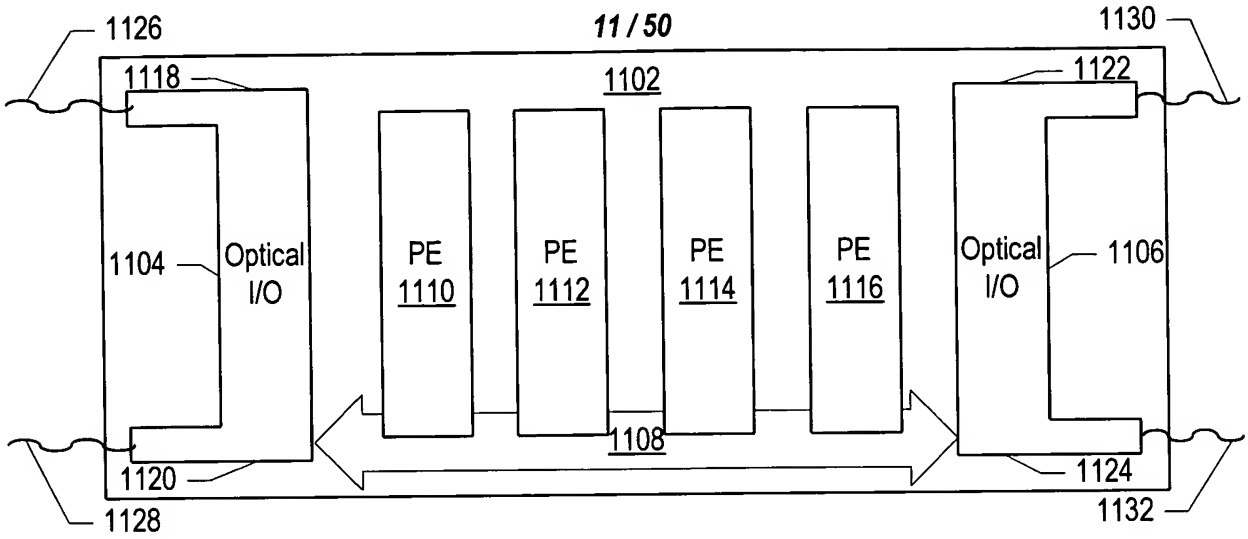

Figure 11A

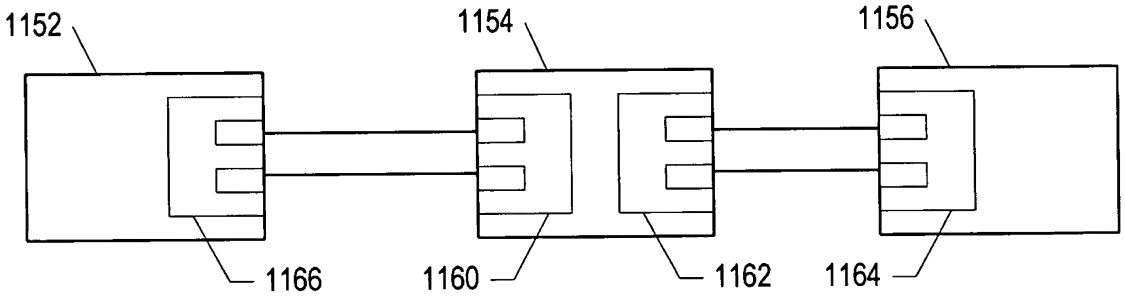

Figure 11B

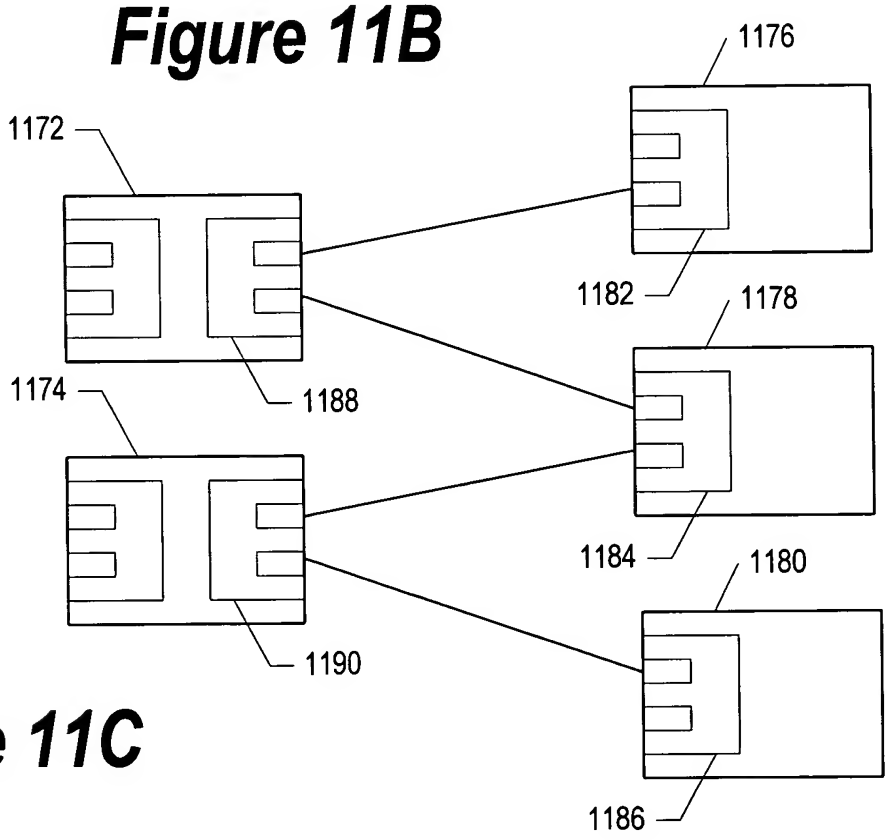

Figure 11C

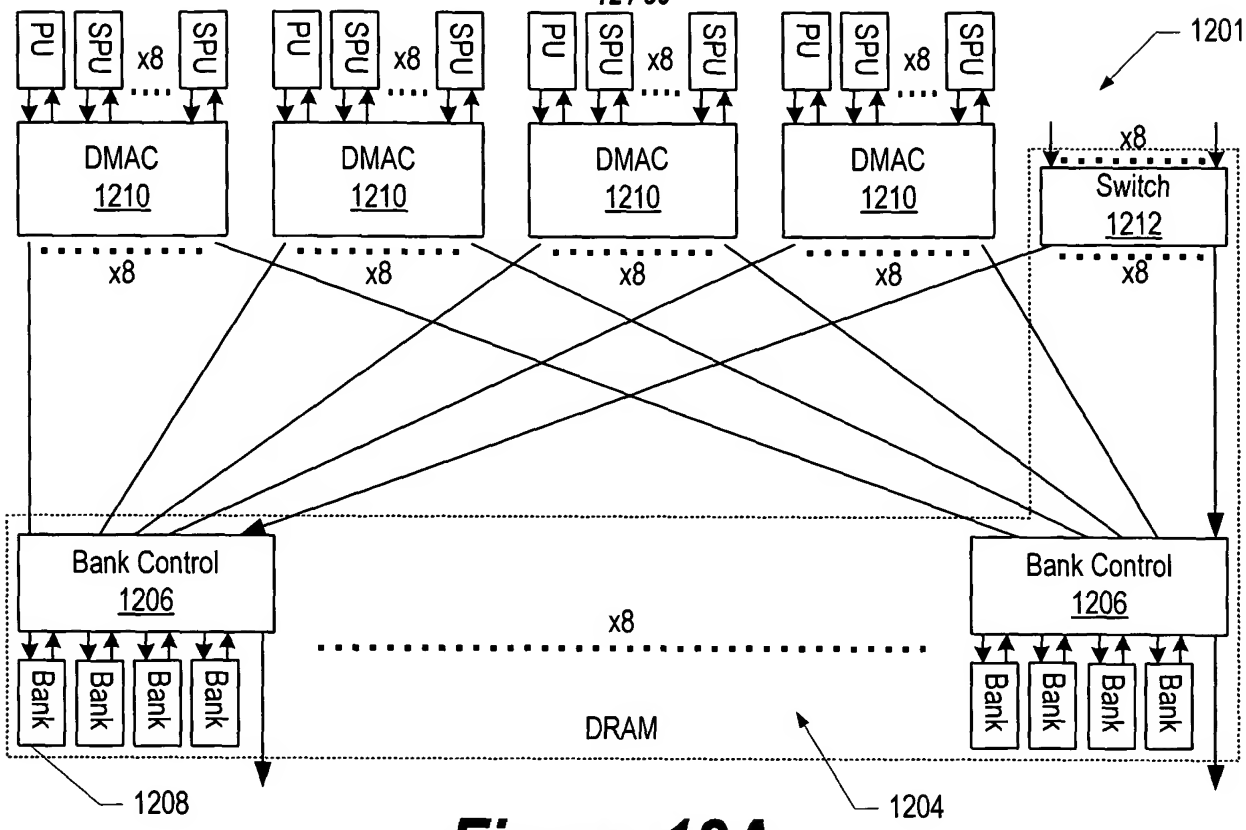

Figure 12A

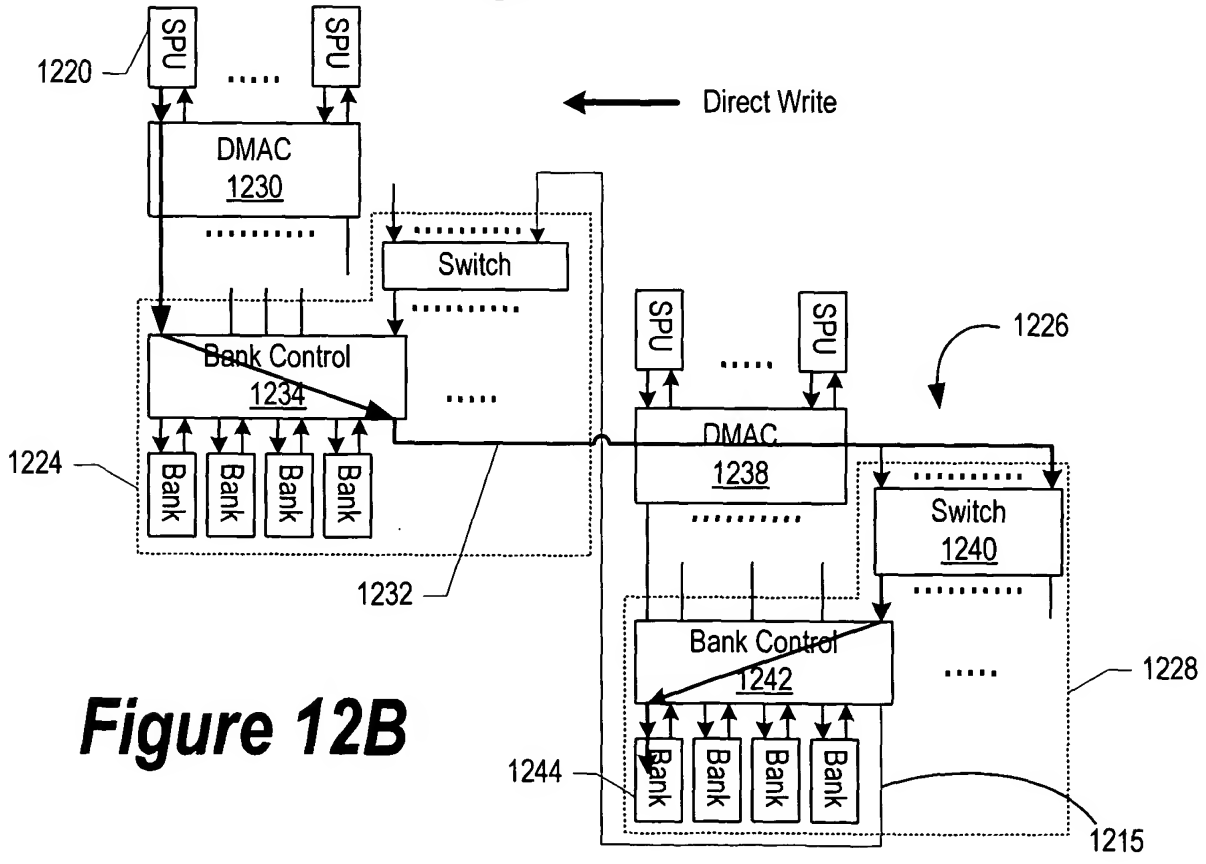

Figure 12B

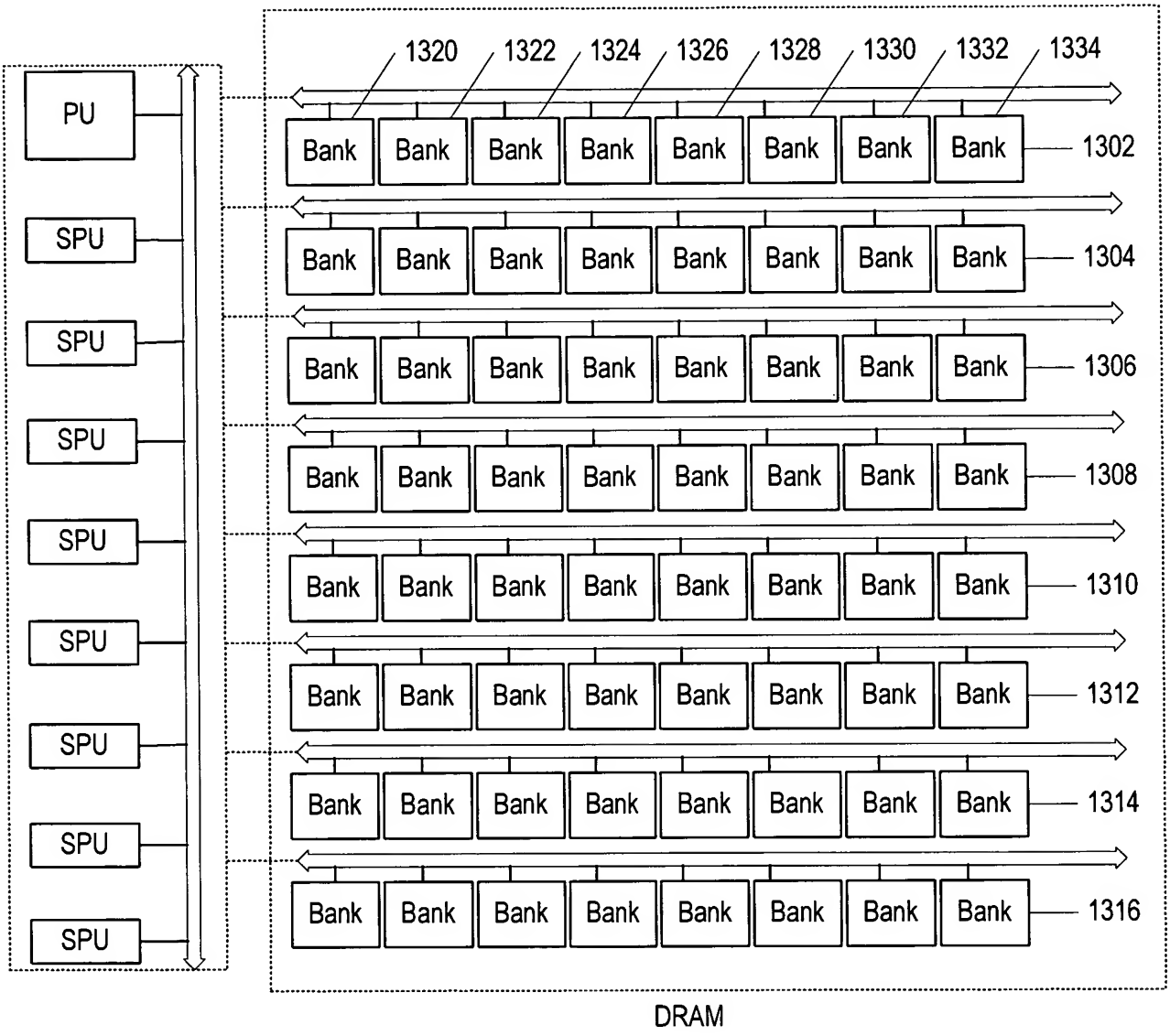
1320
1322
1324
1326
1328
1330
1332
1334
PU
SPU
SPU
SPU
SPU
SPU
SPU
SPU
SPU
Bank
1302
1304
1306
1308
1310
1312
1314
1316
DRAM

Figure 13

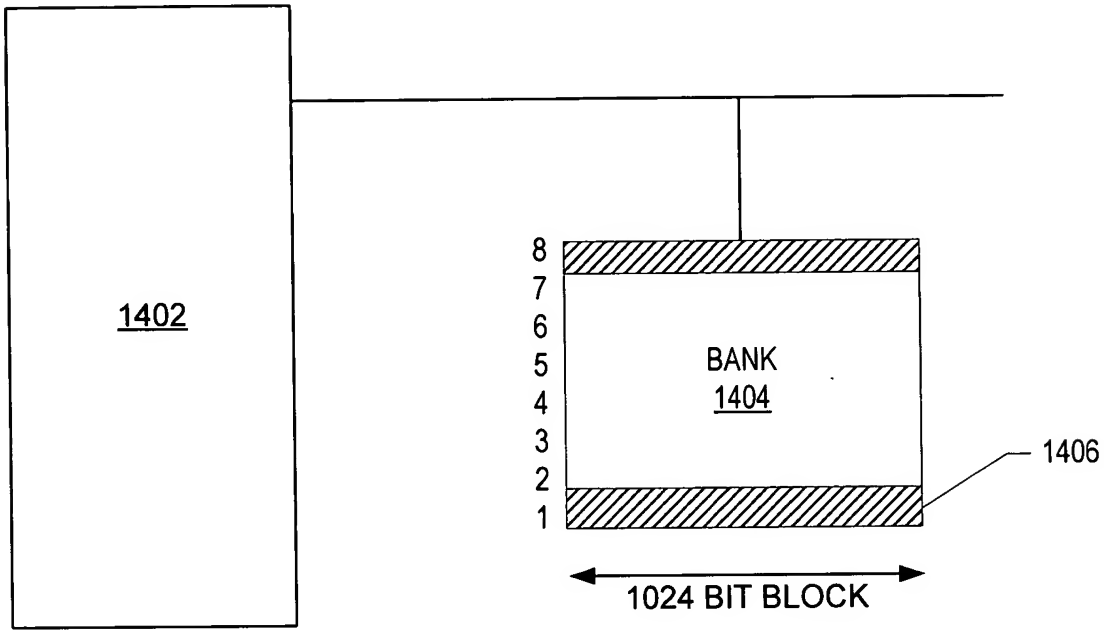

Figure 14A

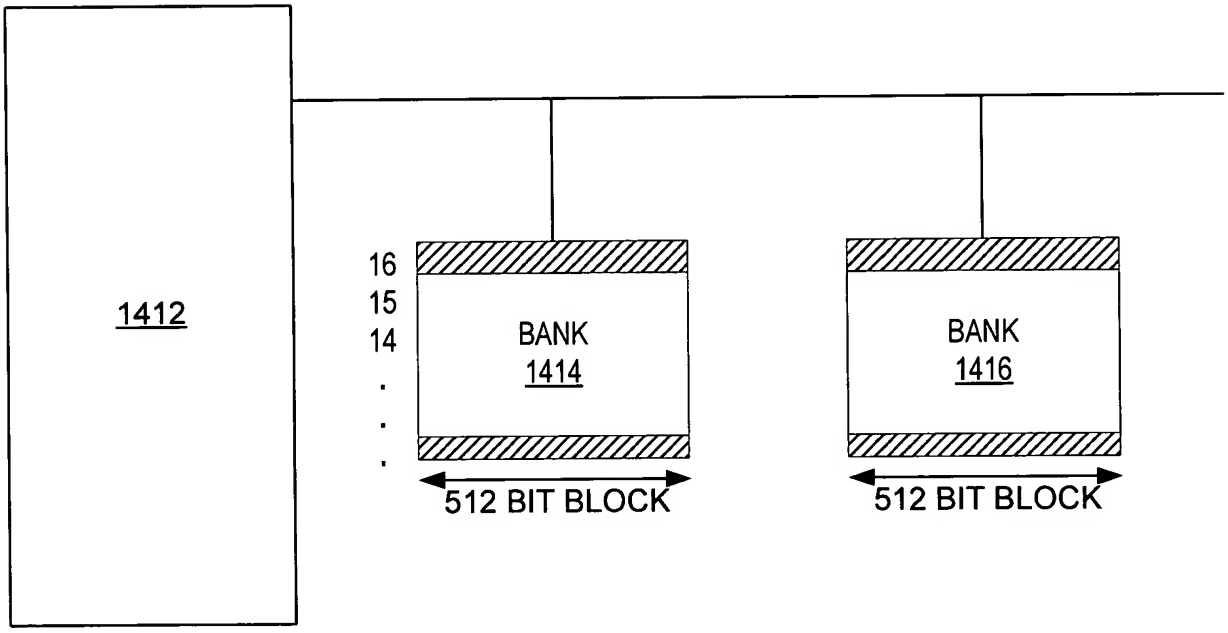

Figure 14B

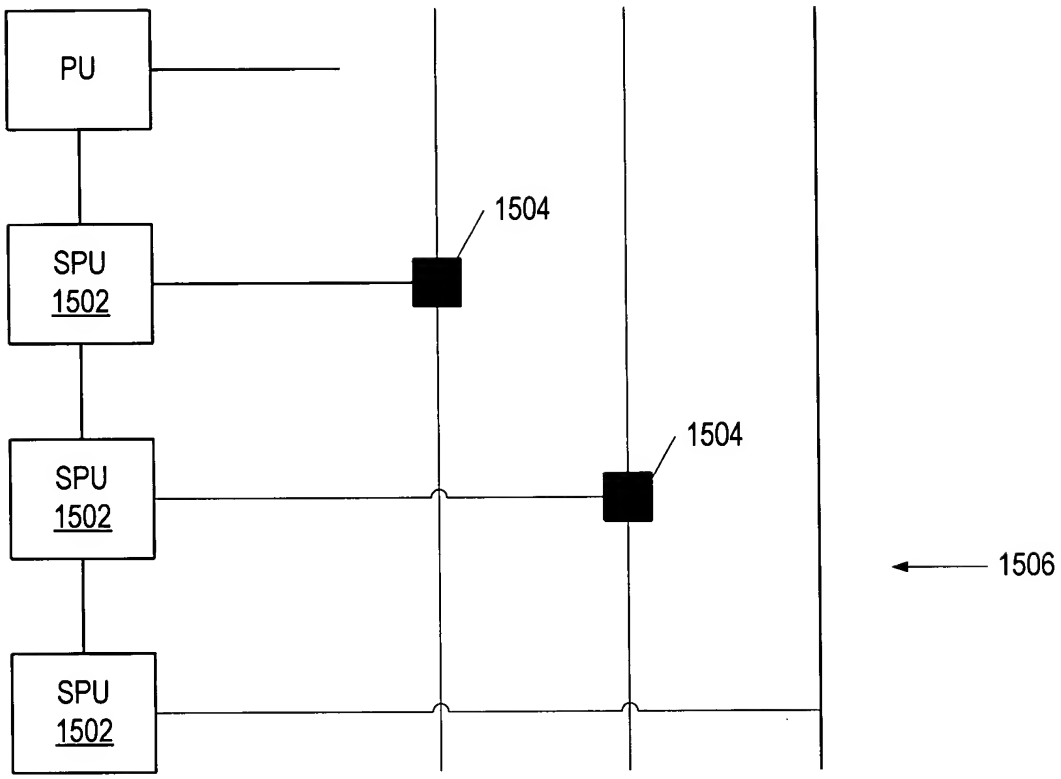

Figure 15

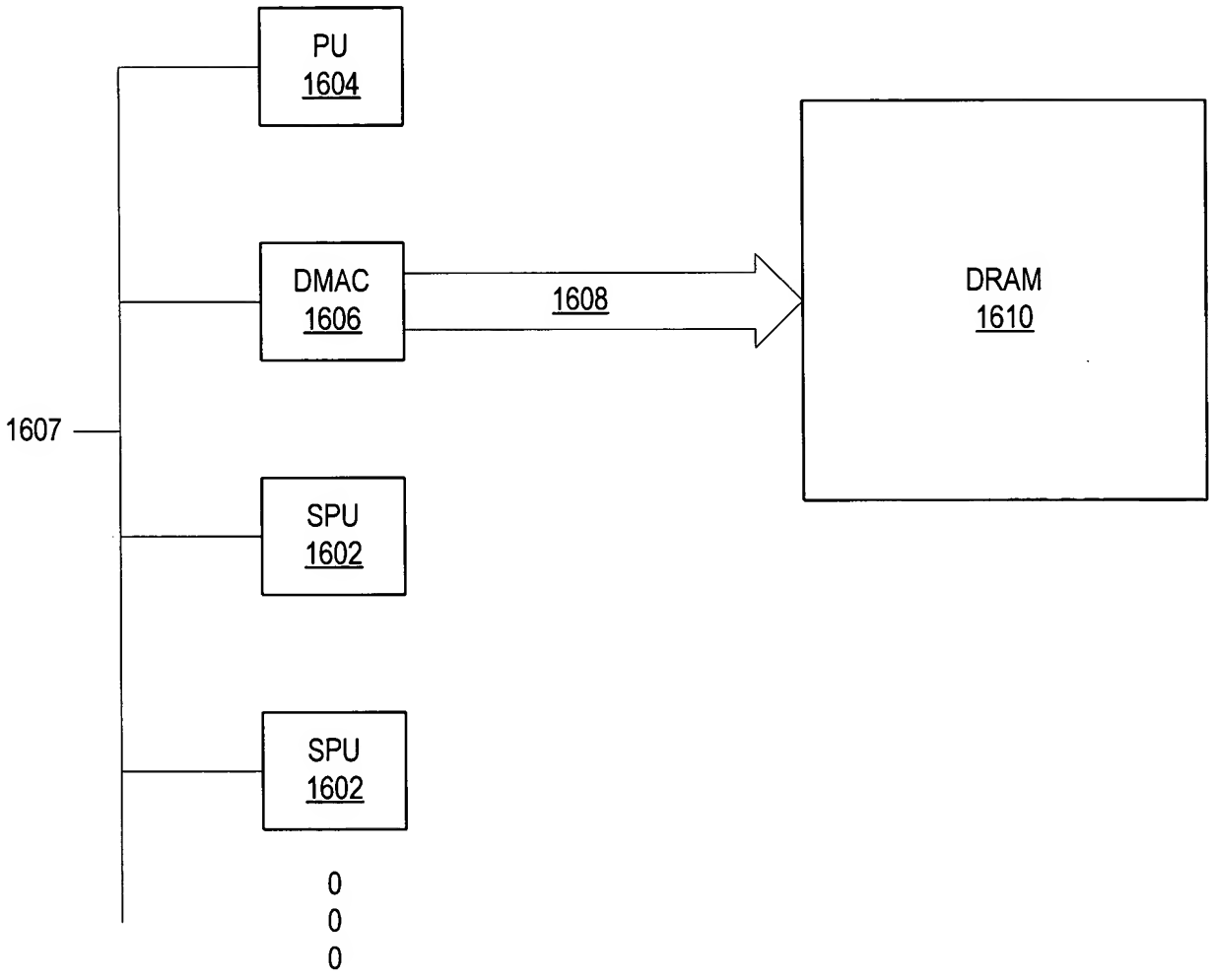

Figure 16

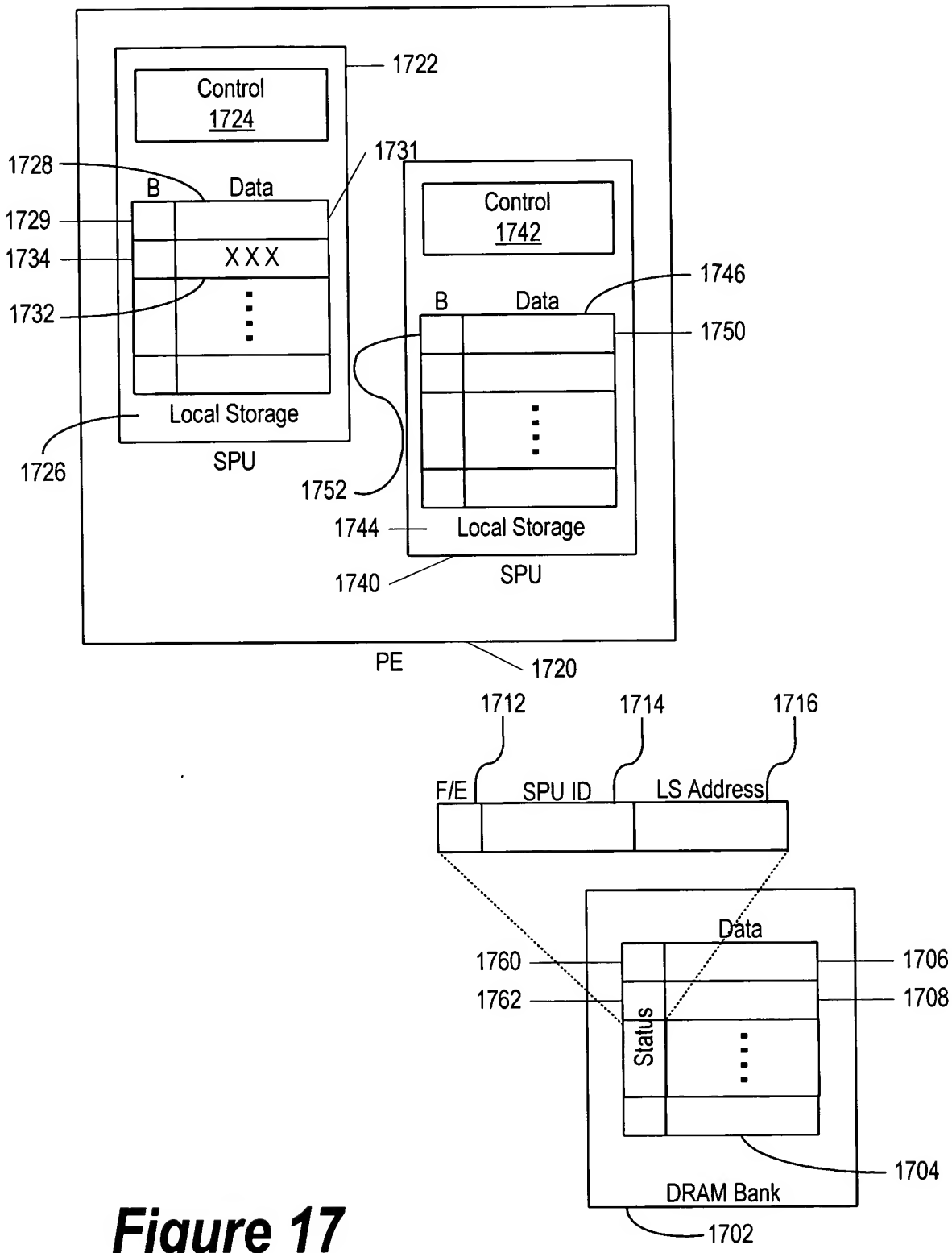
1722
Control
1724
1728
B
Data
1729
1734
XXX
1732
1731
Control
1742
1746
B
Data
1750
Local Storage
1726
SPU
1752
1744
Local Storage
1740
SPU
PE
1720
1712
1714
1716
F/E
SPU ID
LS Address
Data
1760
1762
1706
1708
Status
1704
DRAM Bank
1702

Figure 17

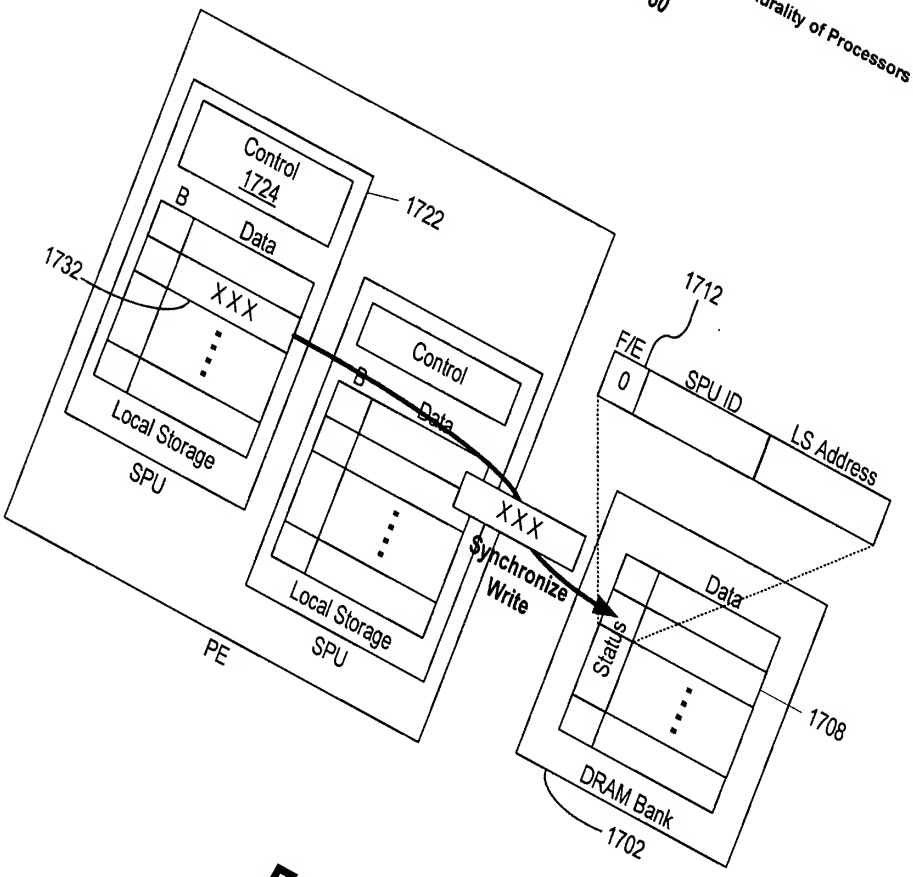
Control
1724
B
Data
XXX
1722
1732
Local Storage
SPU
Control
B
Data
XXX
Local Storage
SPU
PE
1712
F/E
0
SPU ID
LS Address
Synchronize
Write
Data
Status
1708
DRAM Bank
1702

Figure 18

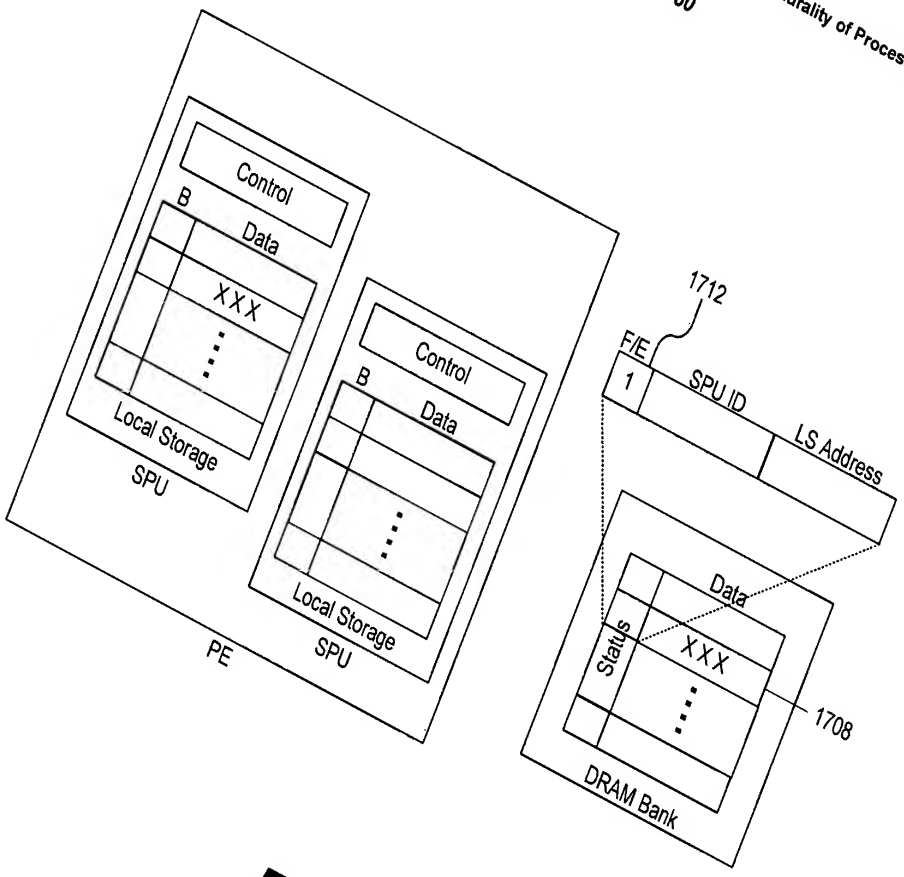
Control
B
Data
XXX
Local Storage
SPU
Control
B
Data
Local Storage
SPU
PE
1712
F/E
1
SPU ID
LS Address
Data
Status
XXX
1708
DRAM Bank

Figure 19

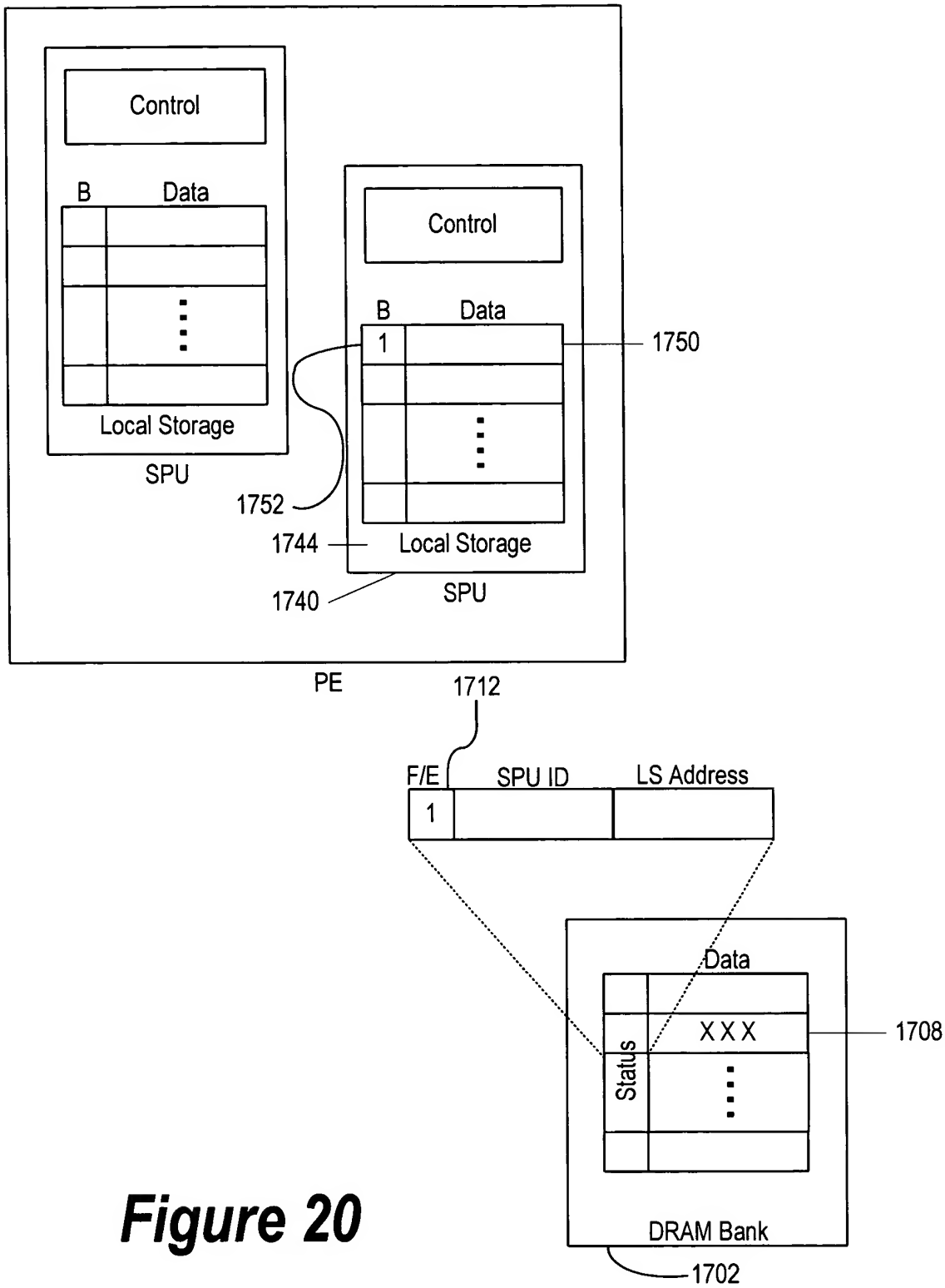
Control
B
Data
Local Storage
SPU
Control
B
Data
1
1750
1752
1744
Local Storage
1740
SPU
PE
1712
F/E
SPU ID
LS Address
1
Data
XXX
Status
1708
DRAM Bank
1702

Figure 20

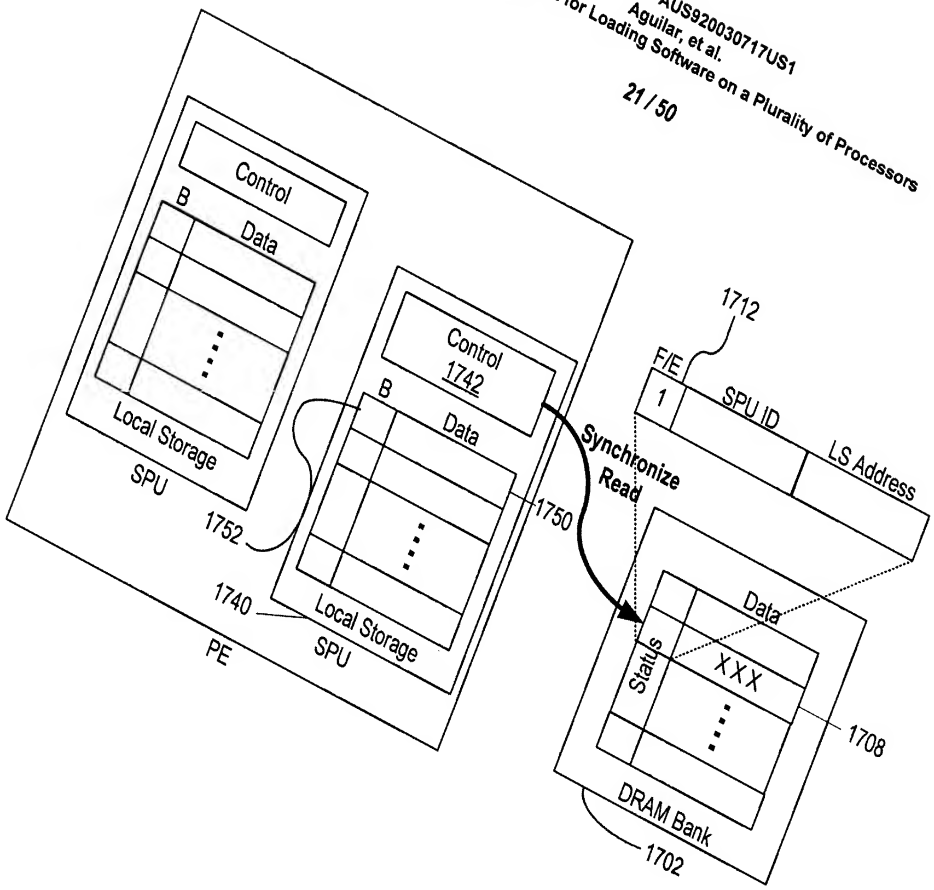
Control
B
Data
Local Storage
SPU
1752
Control
1742
B
Data
1750
1740
Local Storage
SPU
PE
1712
F/E
1
SPU ID
LS Address
Synchronize
Read
Data
Status
XXX
1708
DRAM Bank
1702

Figure 21

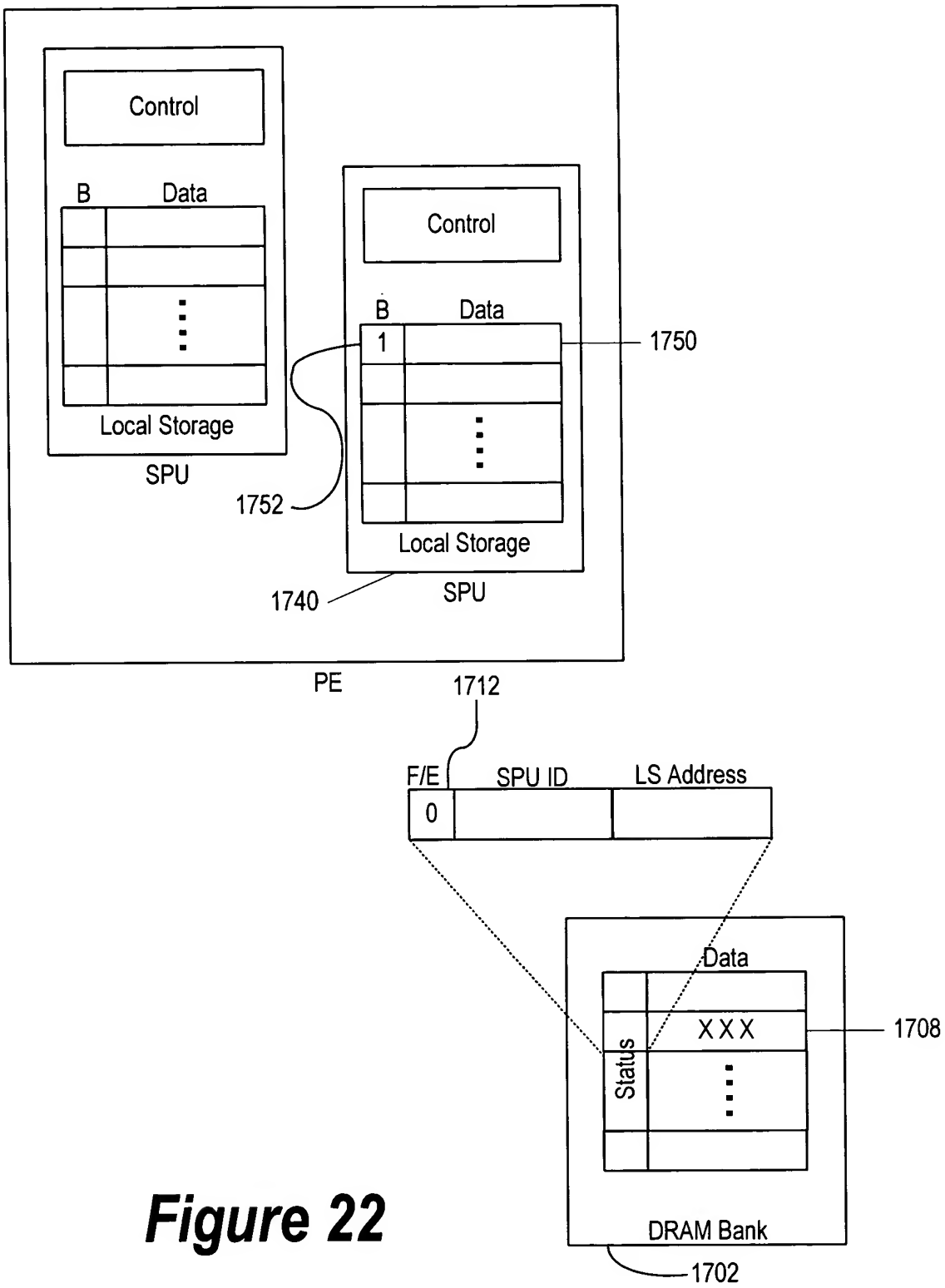
Control
B
Data
Local Storage
SPU
Control
B
Data
1
1750
1752
Local Storage
SPU
1740
PE
1712
F/E
SPU ID
LS Address
0
Data
XXX
1708
Status
DRAM Bank
1702

Figure 22

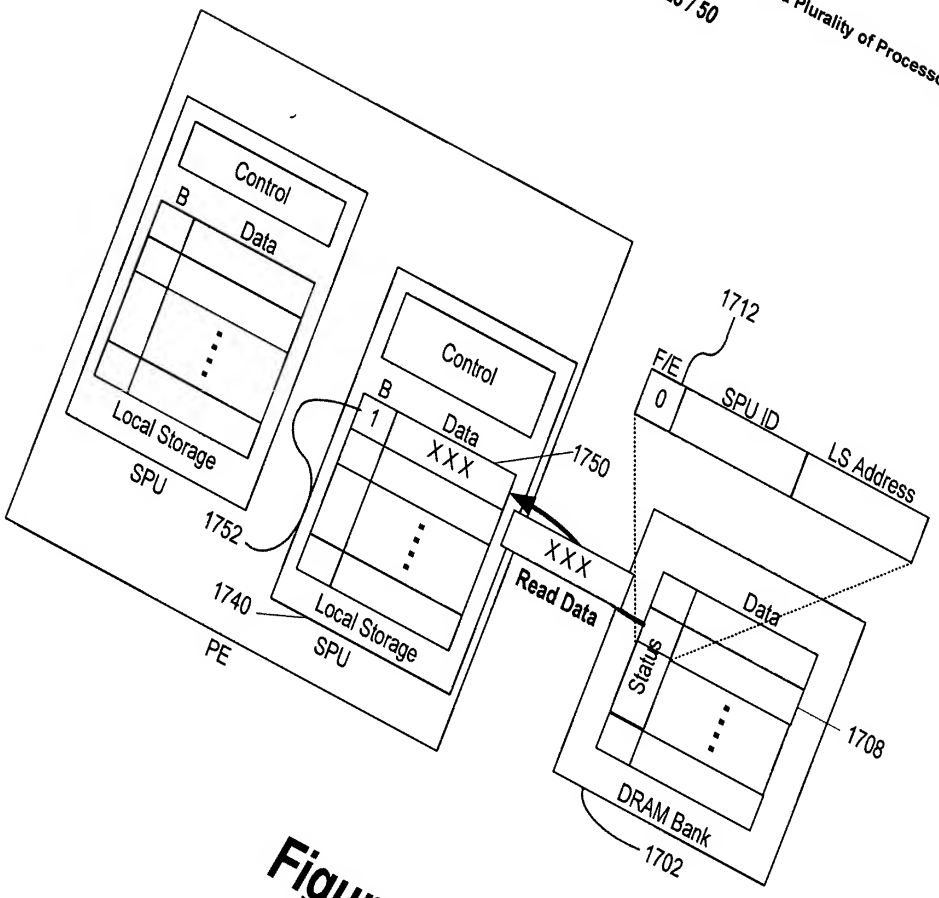
Control
B
Data
Local Storage
SPU
1752
Control
B
1
Data
XXX
1750
1740
Local Storage
SPU
PE
1712
F/E
0
SPU ID
LS Address
XXX
Read Data
Data
Status
1708
DRAM Bank
1702

Figure 23

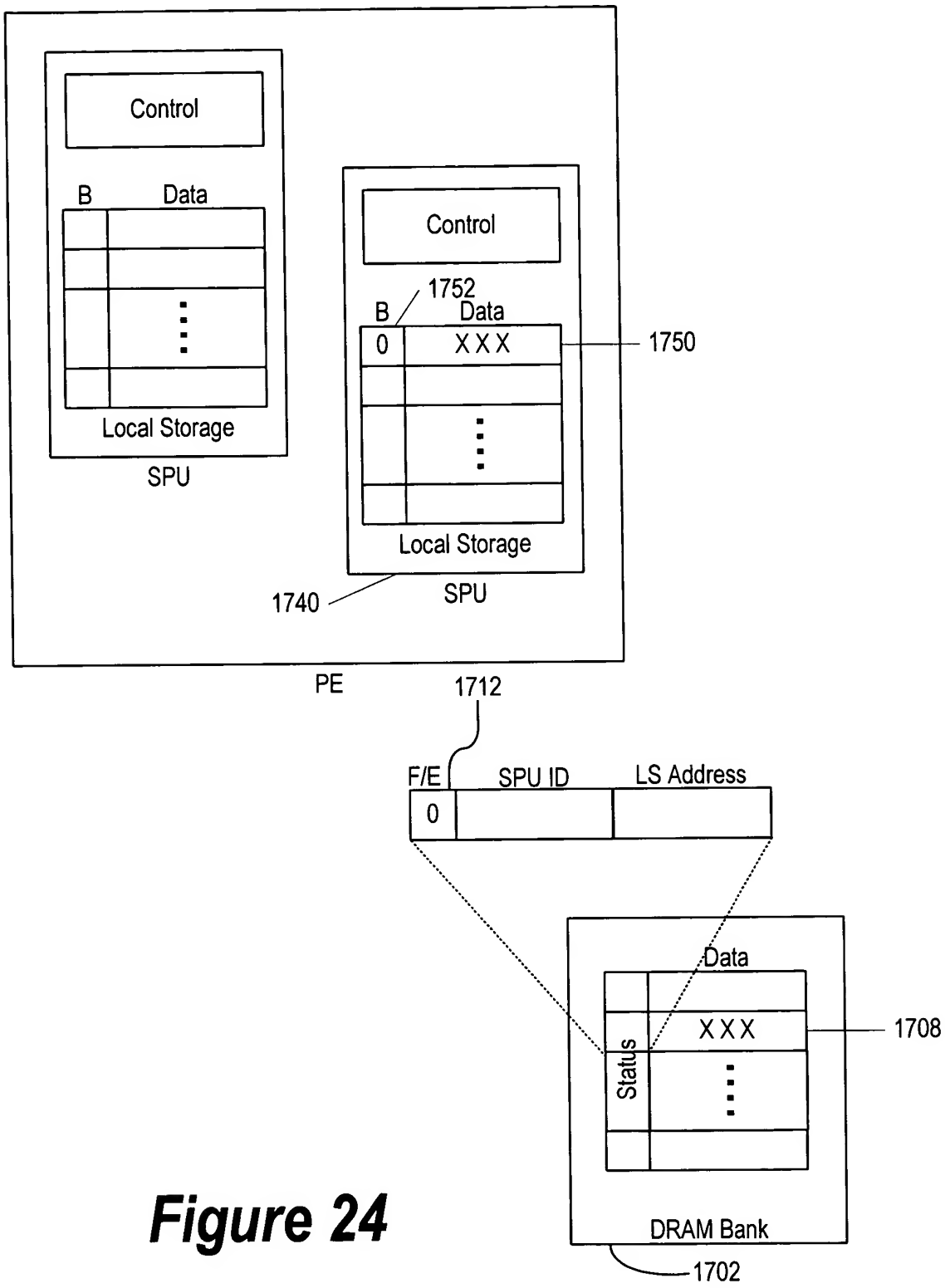
Control
B
Data
Local Storage
SPU
Control
1752
B
Data
0
XXX
1750
Local Storage
SPU
1740
PE
1712
F/E
SPU ID
LS Address
0
Data
XXX
1708
Status
DRAM Bank
1702

Figure 24

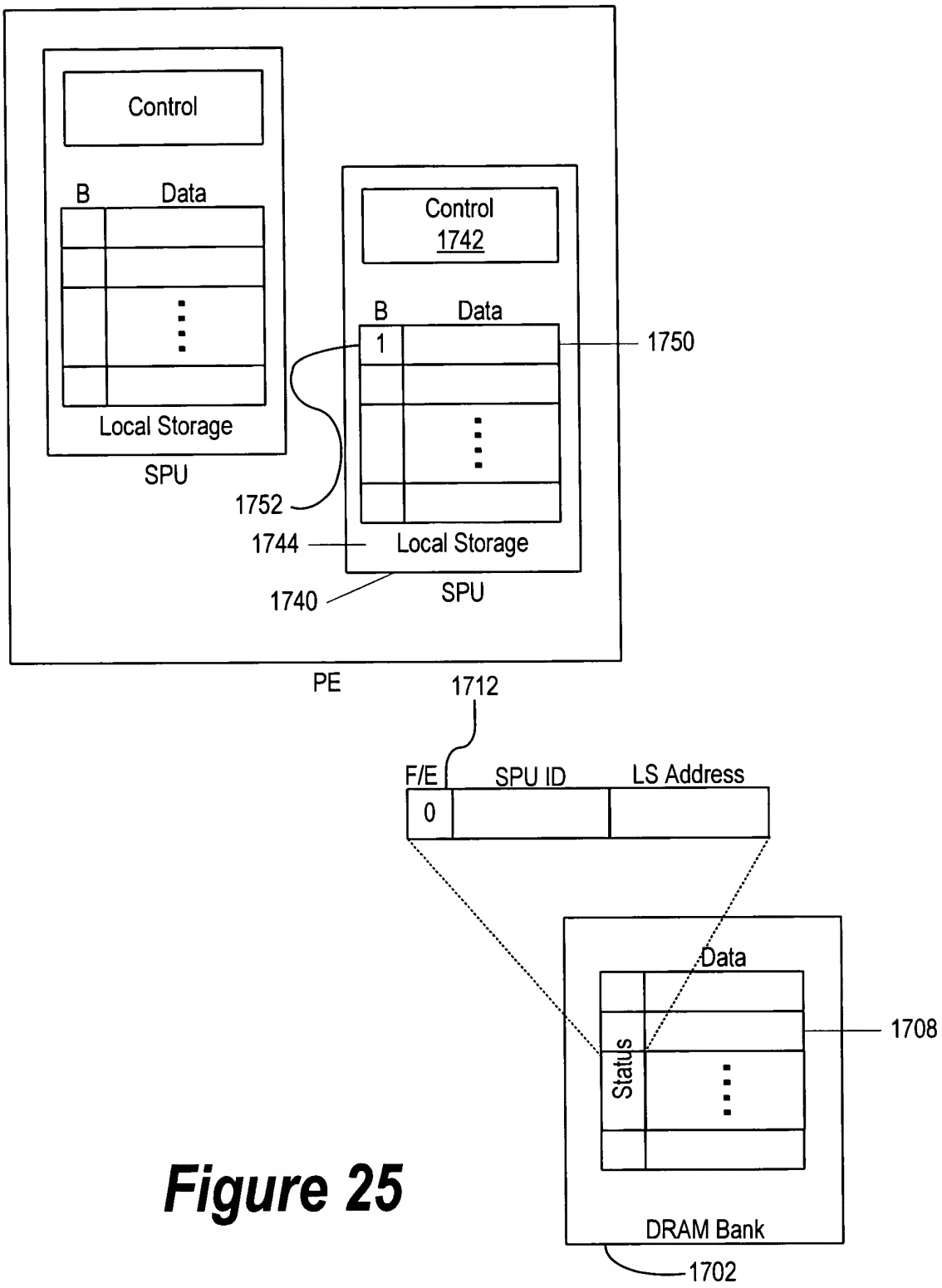
Control
B
Data
Local Storage
SPU
Control
1742
B
Data
1
1750
1752
1744
Local Storage
1740
SPU
PE
1712
F/E
SPU ID
LS Address
0
Data
Status
1708
DRAM Bank
1702

Figure 25

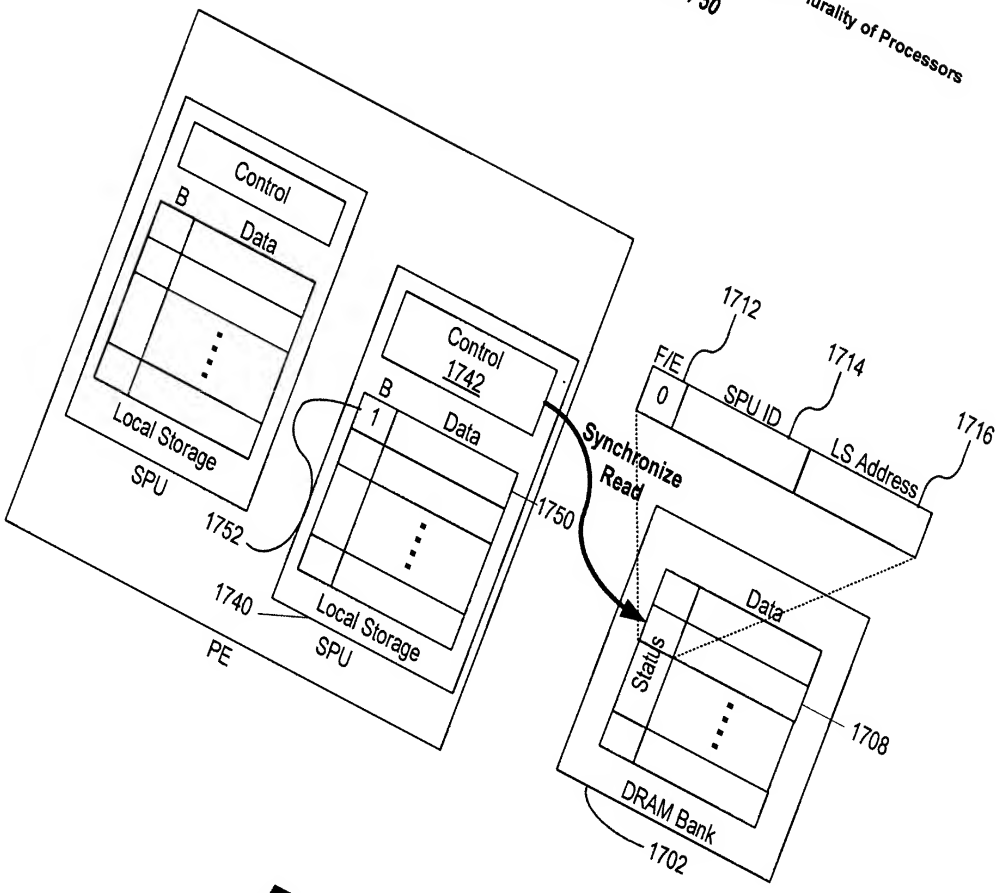
Control
B
Data
Local Storage
SPU
1752
Control
1742
B
1
Data
1750
1740
Local Storage
SPU
PE
1712
F/E
0
1714
SPU ID
LS Address
1716
Synchronize
Read
Data
Status
1708
DRAM Bank
1702

Figure 26

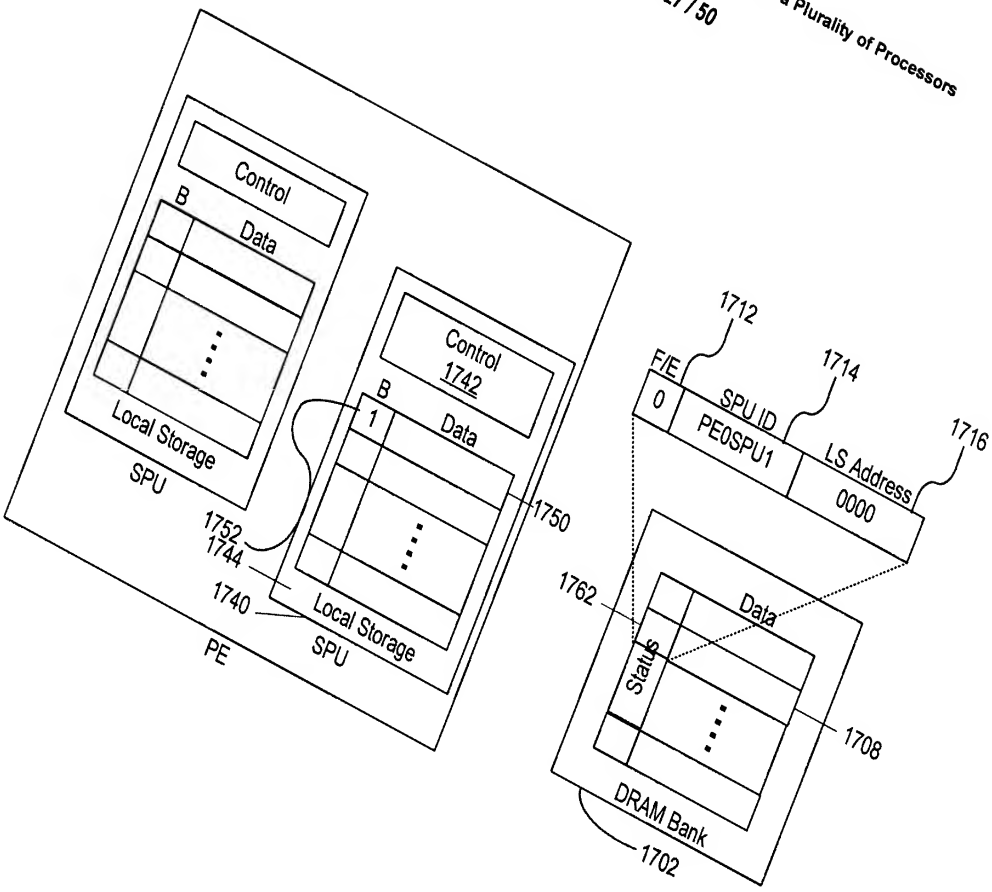
Control
B
Data
Local Storage
SPU
Control
1742
B
1
Data
1750
1752
1744
1740
Local Storage
SPU
PE
1712
F/E
0
1714
SPU ID
PE0SPU1
LS Address
0000
1716
1762
Data
Status
1708
DRAM Bank
1702

Figure 27

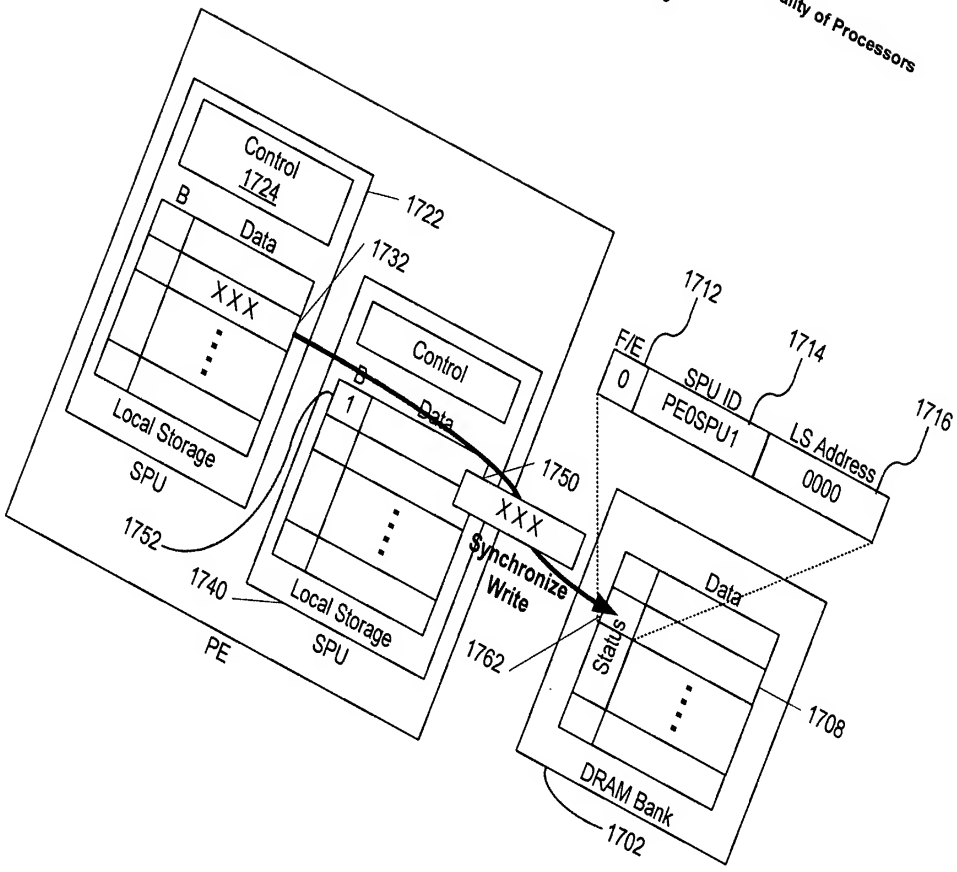
Control
1724
B
Data
XXX
Local Storage
SPU
1722
1732
Control
B
1
Data
Local Storage
SPU
PE
1740
1752
1750
XXX
Synchronize
Write
1762
1712
F/E
0
SPU ID
PE0SPU1
1714
LS Address
0000
1716
Data
Status
1708
DRAM Bank
1702

Figure 28

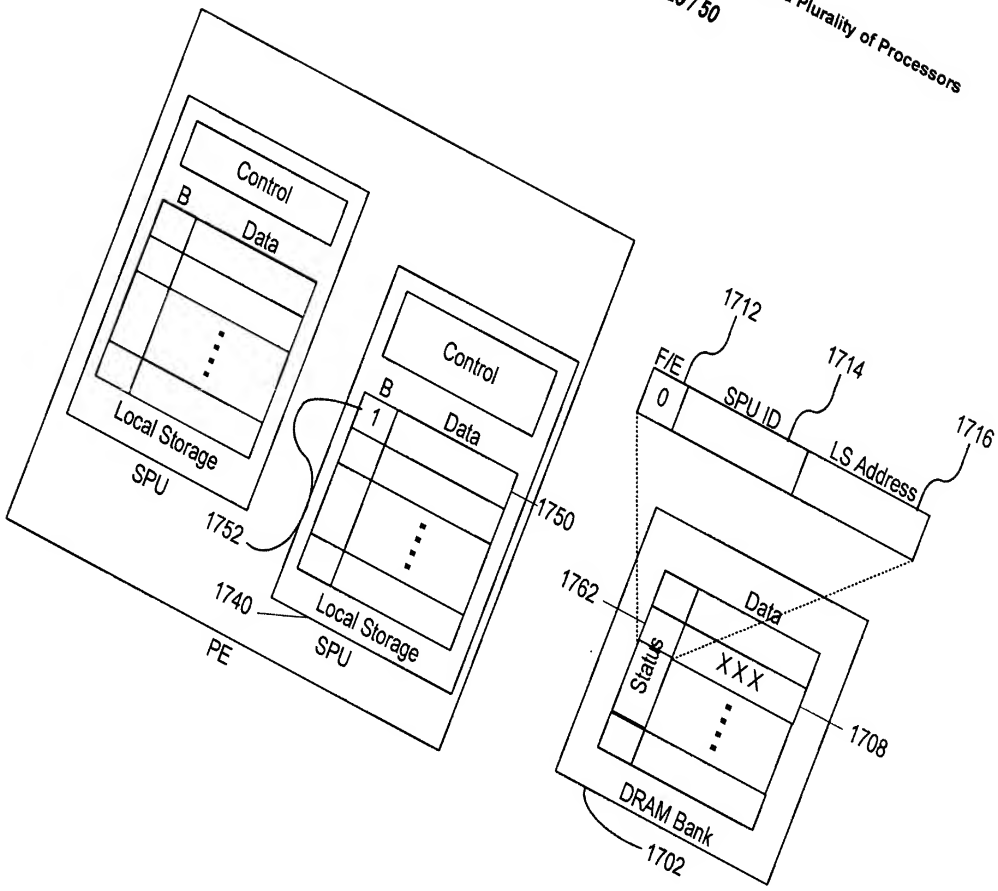
Control
B
Data
Local Storage
SPU
1752
Control
B
1
Data
1750
1740
Local Storage
SPU
PE
1712
F/E
0
1714
SPU ID
1716
LS Address
1762
Data
Status
XXX
1708
DRAM Bank
1702

Figure 29

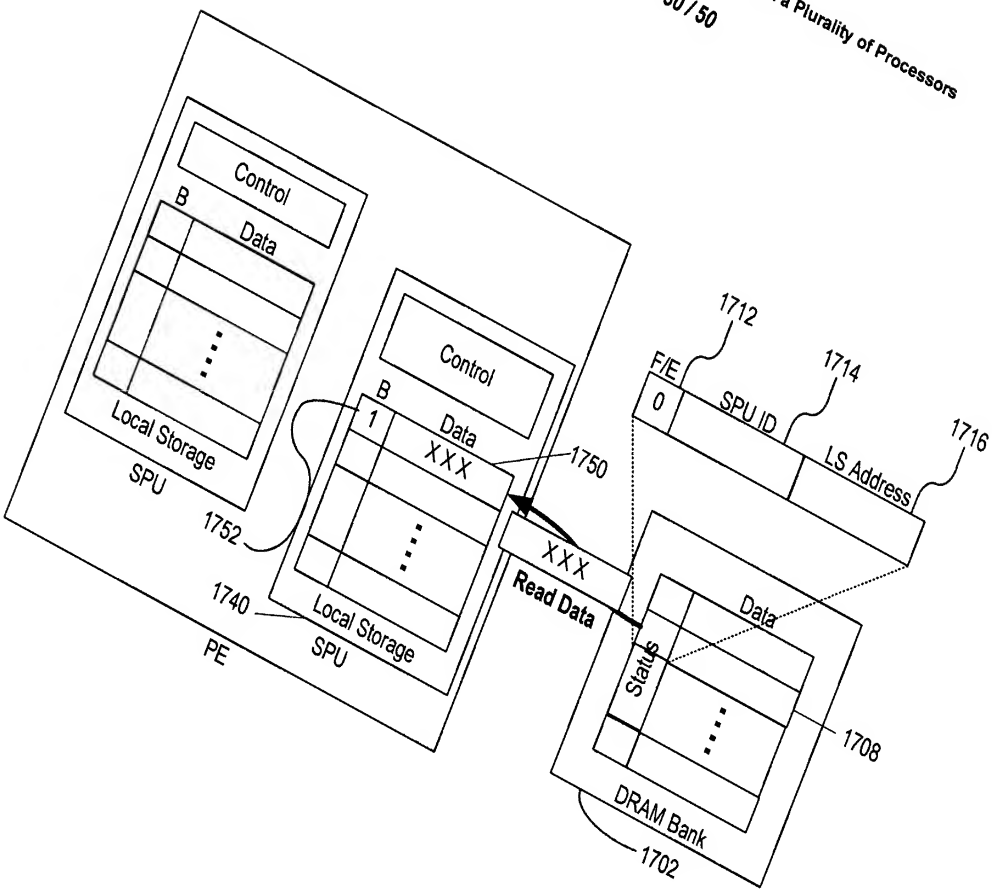
Control
B
Data
Local Storage
SPU
1752
Control
B
1
Data
XXX
1750
1740
Local Storage
SPU
PE
1712
F/E
0
1714
SPU ID
1716
LS Address
XXX
Read Data
Data
Status
1708
DRAM Bank
1702

Figure 30

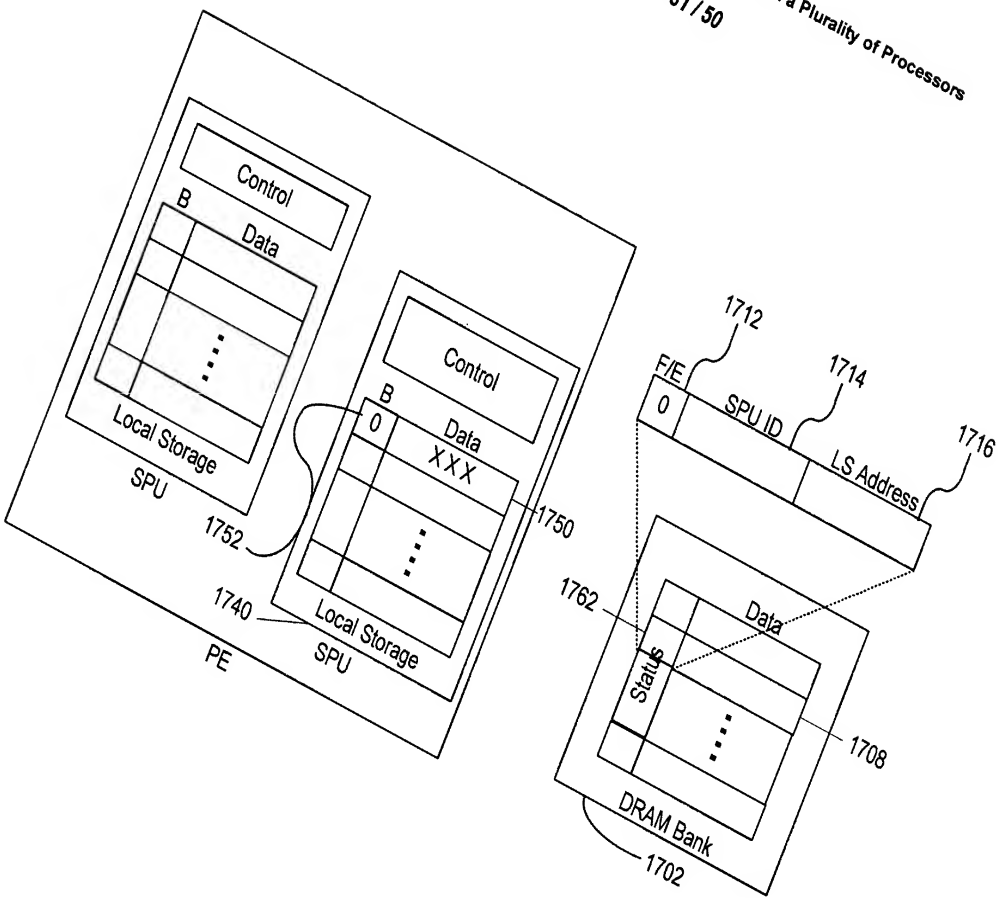
Control
B
Data
Local Storage
SPU
1752
Control
B
0
Data
XXX
1750
1740
Local Storage
SPU
PE
1712
F/E
1714
0
SPU ID
1716
LS Address
1762
Data
Status
1708
DRAM Bank
1702

Figure 31

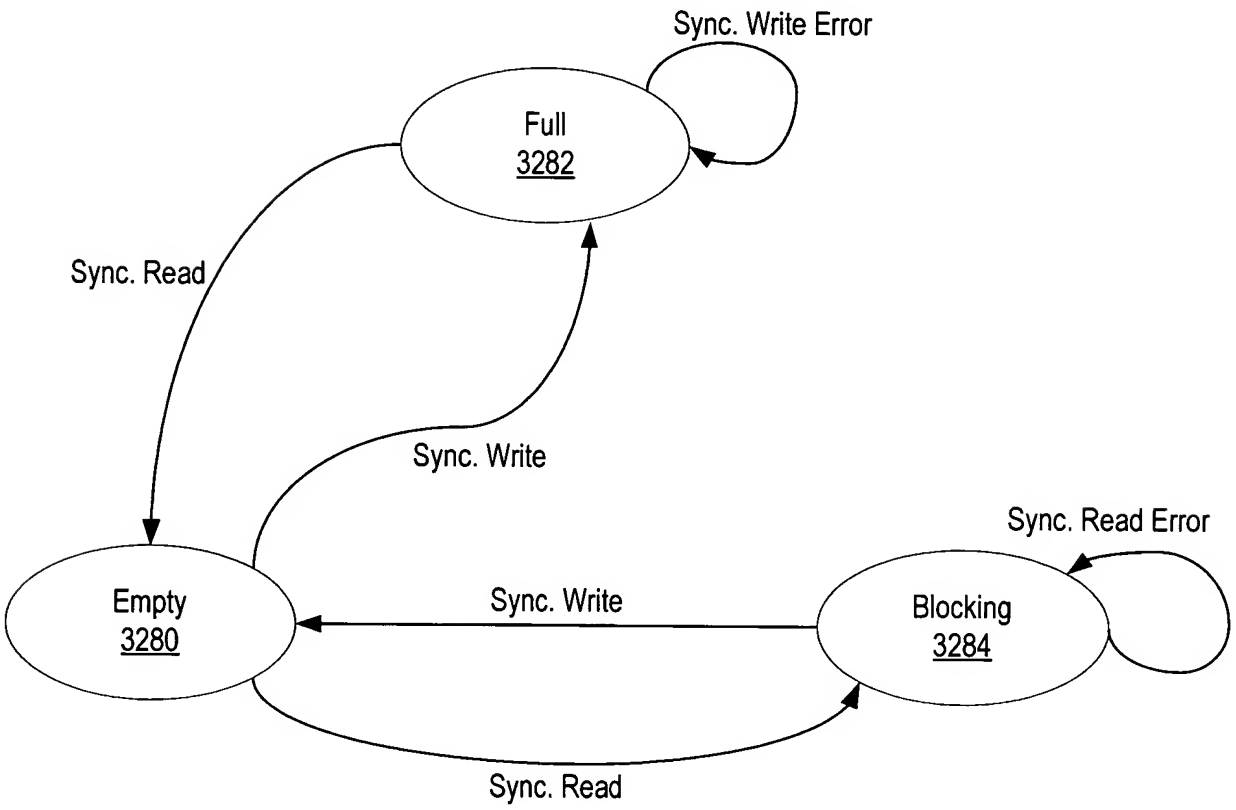
Sync. Write Error
Full
3282
Sync. Read
Sync. Write
Sync. Read Error
Empty
3280
Sync. Write
Blocking
3284
Sync. Read

Figure 32

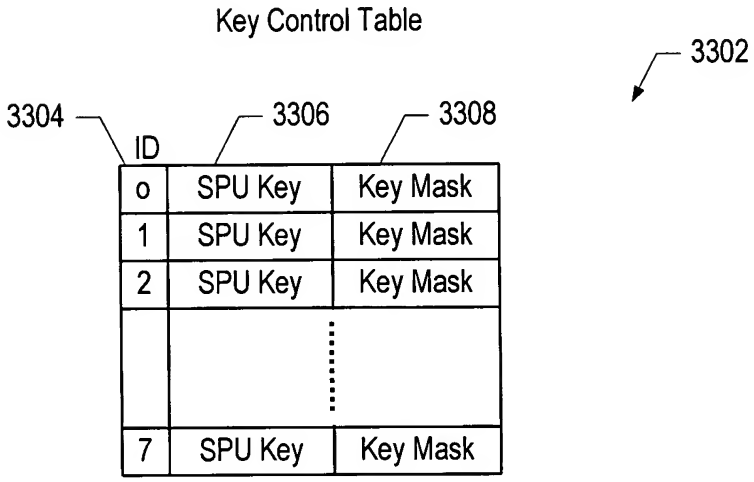
Key Control Table
3302
3304
3306
3308
ID
0
SPU Key
Key Mask
1
SPU Key
Key Mask
2
SPU Key
Key Mask
7
SPU Key
Key Mask

Figure 33

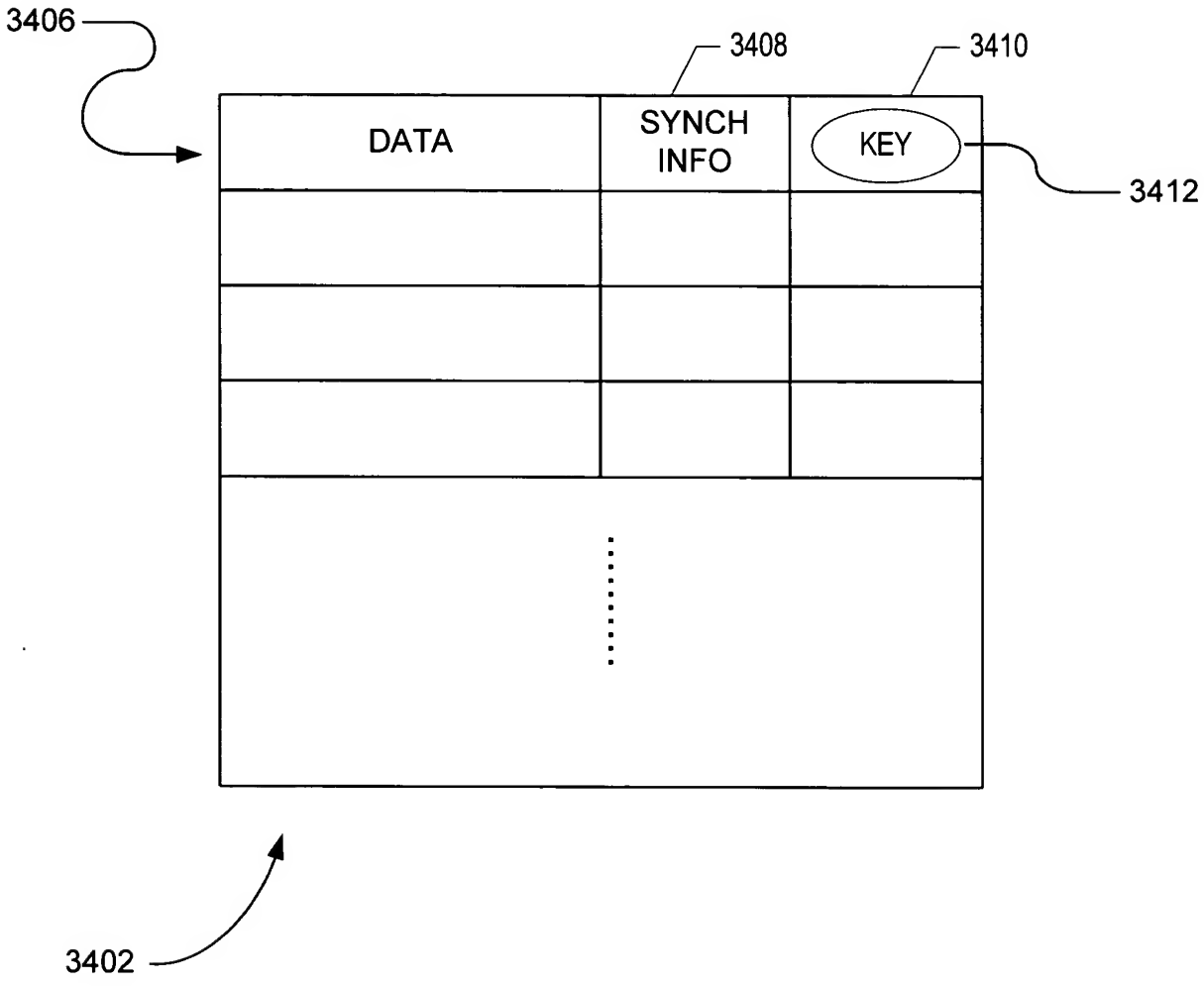

Figure 34

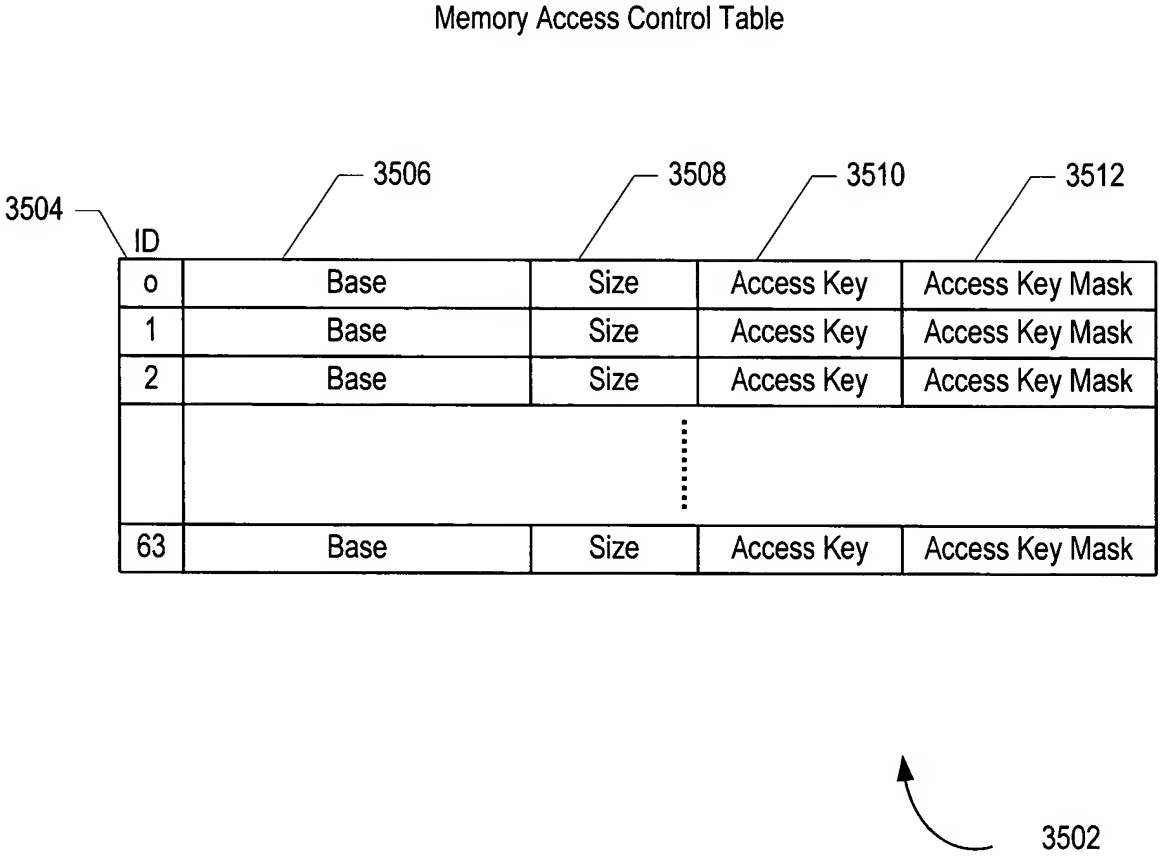
Memory Access Control Table
3504
ID
3506
3508
3510
3512
0
Base
Size
Access Key
Access Key Mask
1
Base
Size
Access Key
Access Key Mask
2
Base
Size
Access Key
Access Key Mask
63
Base
Size
Access Key
Access Key Mask
3502

Figure 35

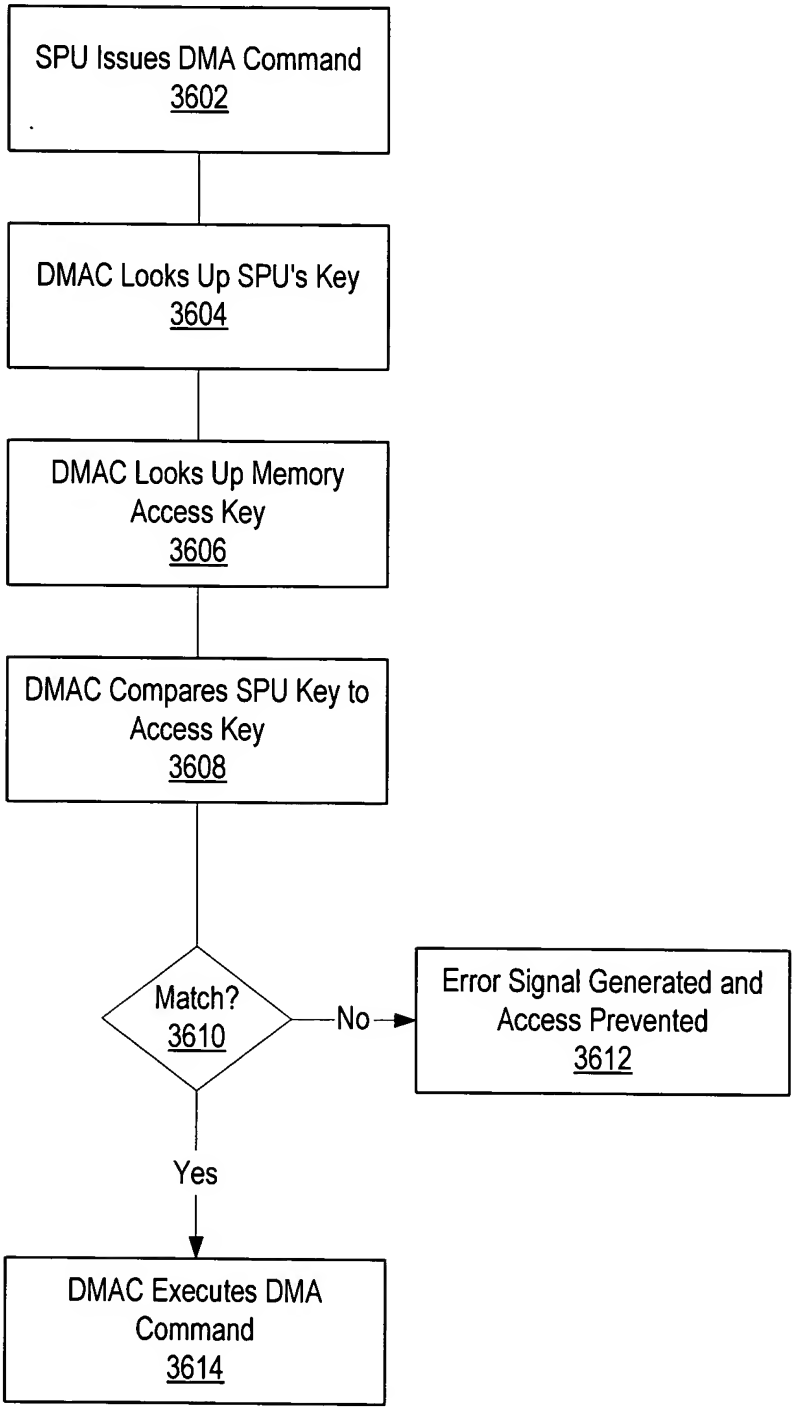
SPU Issues DMA Command
3602
DMAC Looks Up SPU's Key
3604
DMAC Looks Up Memory Access Key
3606
DMAC Compares SPU Key to Access Key
3608
Match?
3610
No
Error Signal Generated and Access Prevented
3612
Yes
DMAC Executes DMA Command
3614

Figure 36

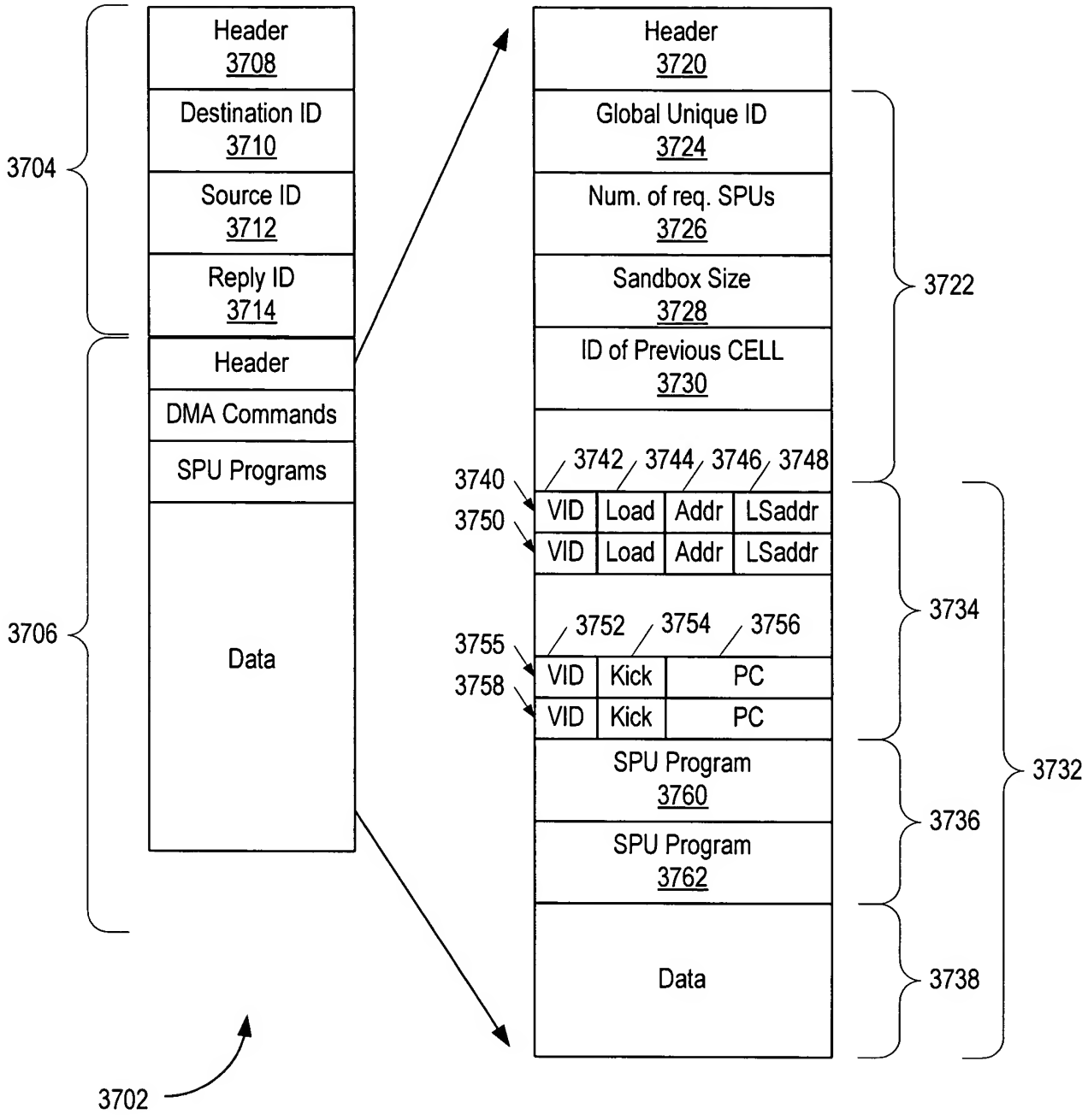
Header
3708
Destination ID
3710
Source ID
3712
Reply ID
3714
3704
Header
DMA Commands
SPU Programs
Data
3706
3702
Header
3720
Global Unique ID
3724
Num. of req. SPUs
3726
Sandbox Size
3728
ID of Previous CELL
3730
3722
3742
3744
3746
3748
3740
VID
Load
Addr
LSaddr
3750
VID
Load
Addr
LSaddr
3734
3752
3754
3756
3755
VID
Kick
PC
3758
VID
Kick
PC
SPU Program
3760
3736
SPU Program
3762
Data
3738
3732

Figure 37

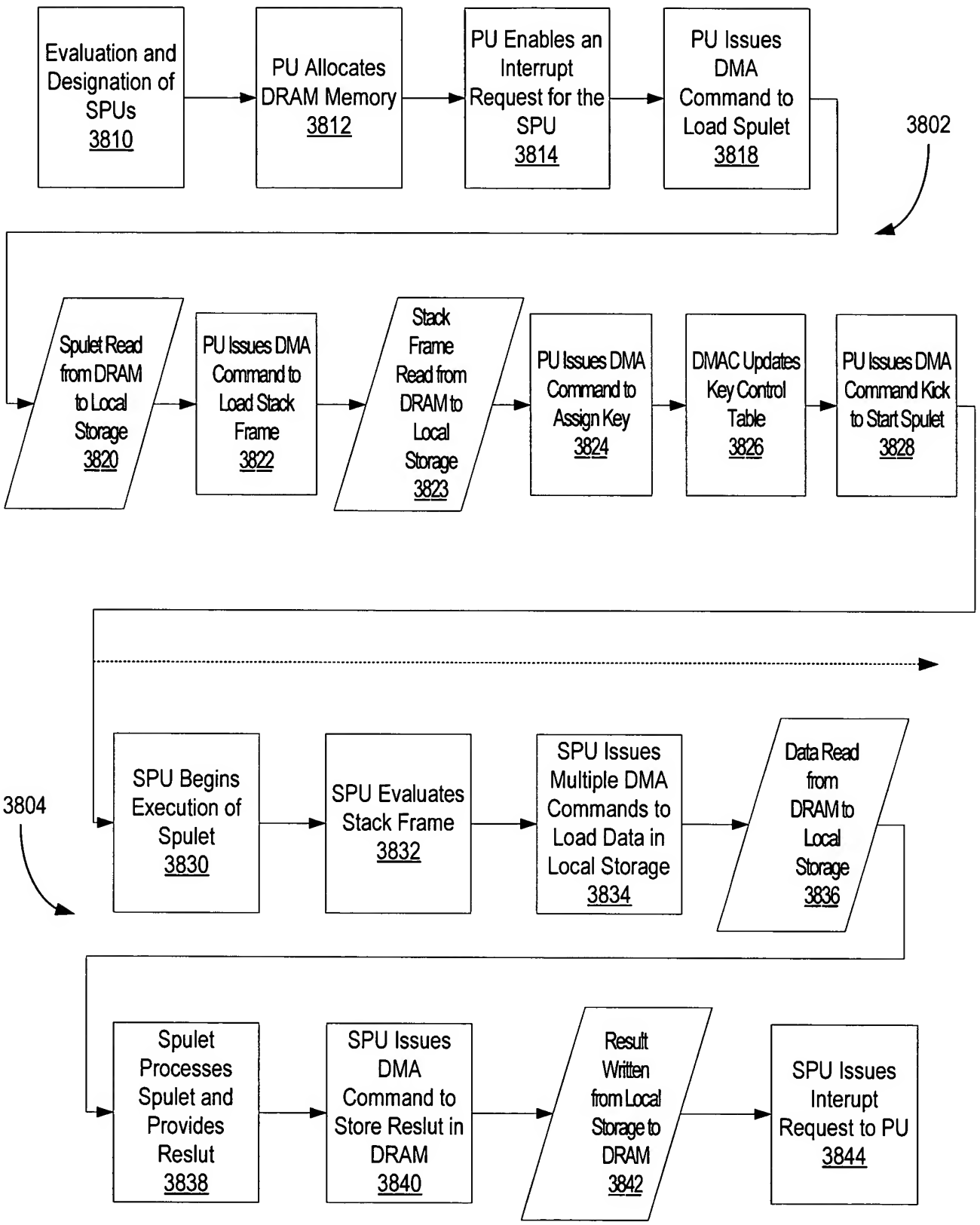
Evaluation and Designation of SPUs 3810
PU Allocates DRAM Memory 3812
PU Enables an Interrupt Request for the SPU 3814
PU Issues DMA Command to Load Spulet 3818
3802
Spulet Read from DRAM to Local Storage 3820
PU Issues DMA Command to Load Stack Frame 3822
Stack Frame Read from DRAM to Local Storage 3823
PU Issues DMA Command to Assign Key 3824
DMAC Updates Key Control Table 3826
PU Issues DMA Command Kick to Start Spulet 3828
3804
SPU Begins Execution of Spulet 3830
SPU Evaluates Stack Frame 3832
SPU Issues Multiple DMA Commands to Load Data in Local Storage 3834
Data Read from DRAM to Local Storage 3836
Spulet Processes Spulet and Provides Reslut 3838
SPU Issues DMA Command to Store Reslut in DRAM 3840
Result Written from Local Storage to DRAM 3842
SPU Issues Interupt Request to PU 3844

Figure 38

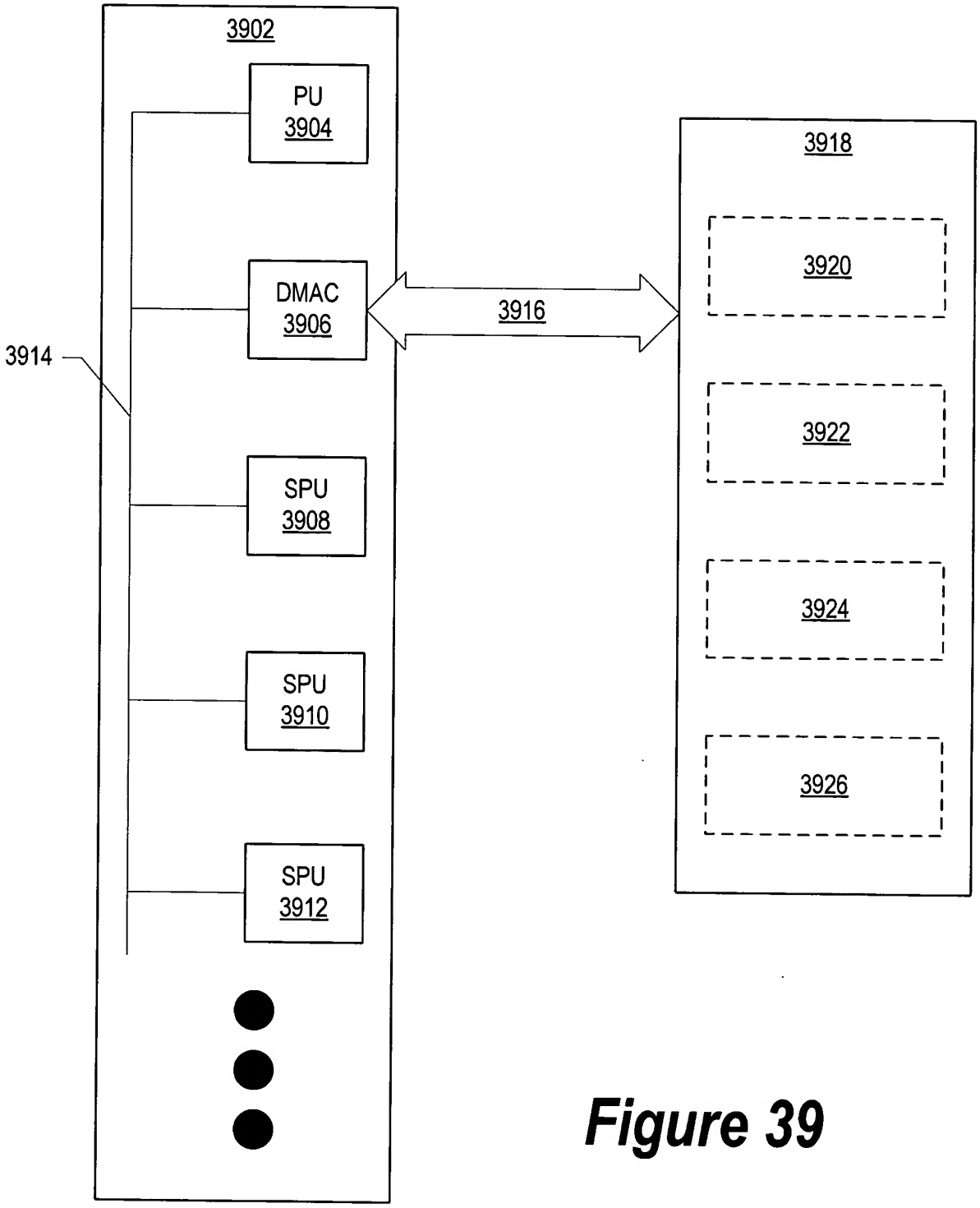
3902
PU
3904
DMAC
3906
3914
SPU
3908
SPU
3910
SPU
3912
3916
3918
3920
3922
3924
3926

Figure 39

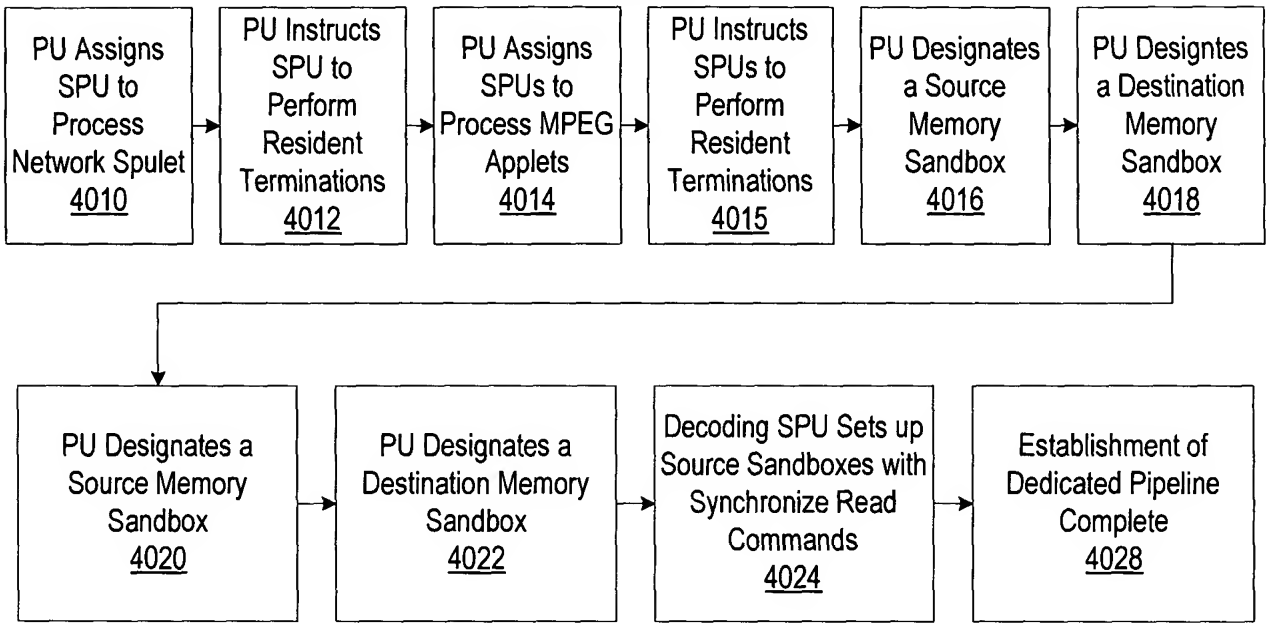

Figure 40A

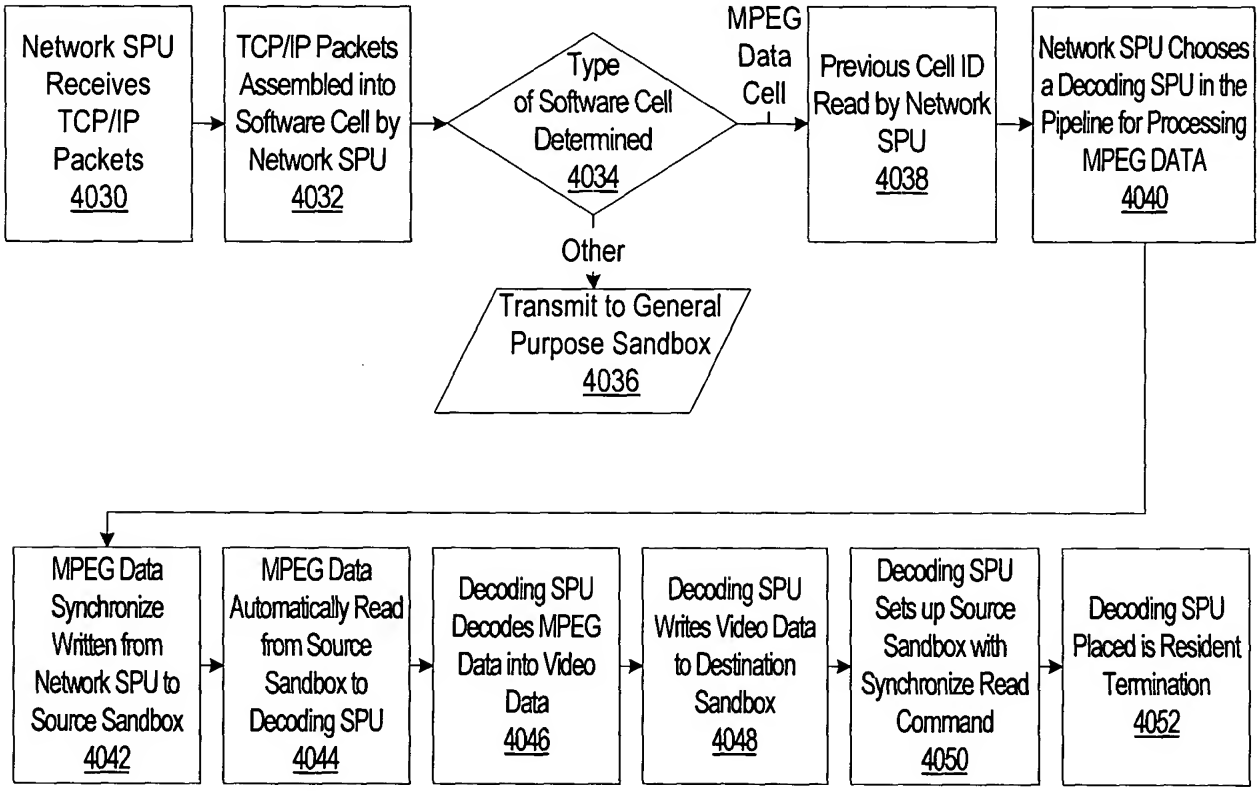

Figure 40B

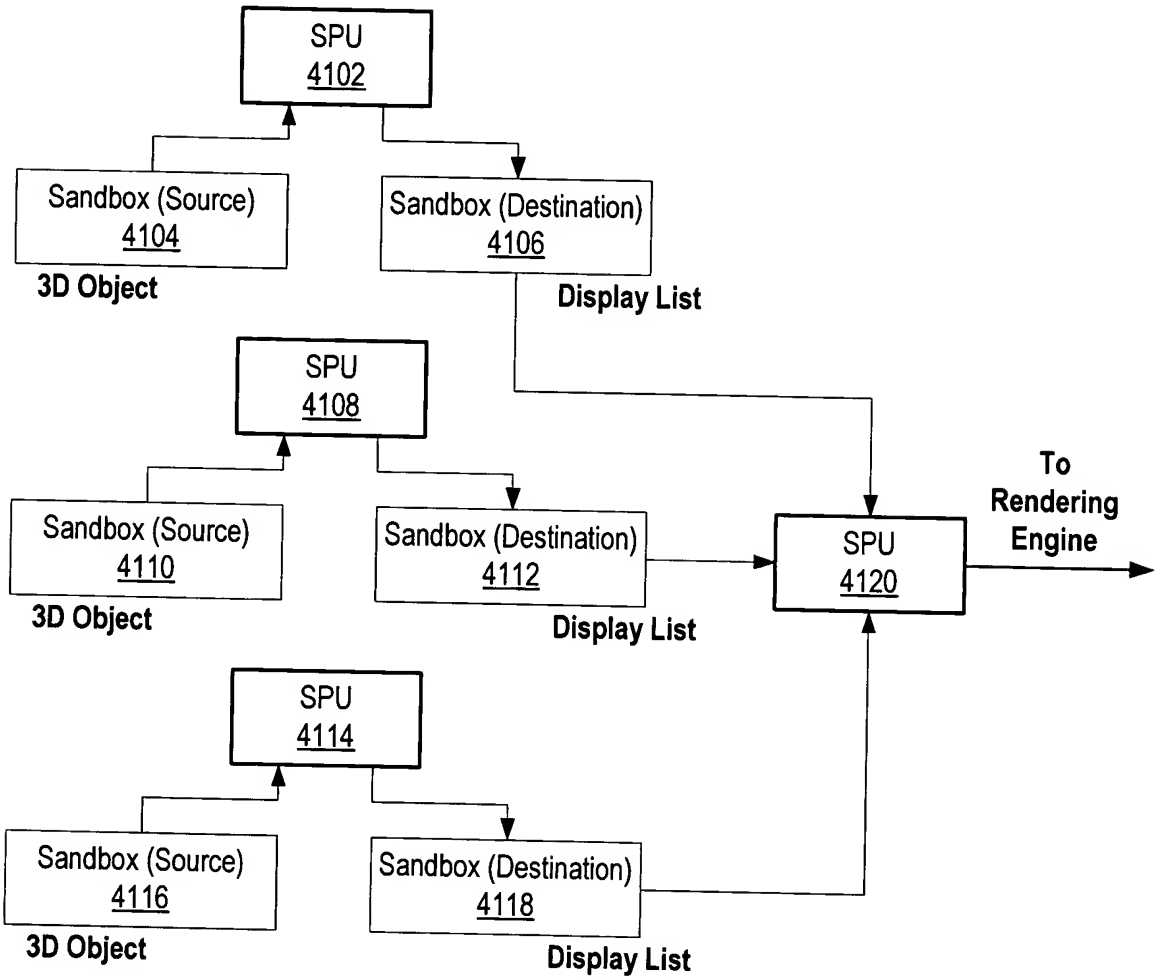
SPU
4102
Sandbox (Source)
4104
3D Object
Sandbox (Destination)
4106
Display List
SPU
4108
Sandbox (Source)
4110
3D Object
Sandbox (Destination)
4112
Display List
SPU
4120
To
Rendering
Engine
SPU
4114
Sandbox (Source)
4116
3D Object
Sandbox (Destination)
4118
Display List

Figure 41

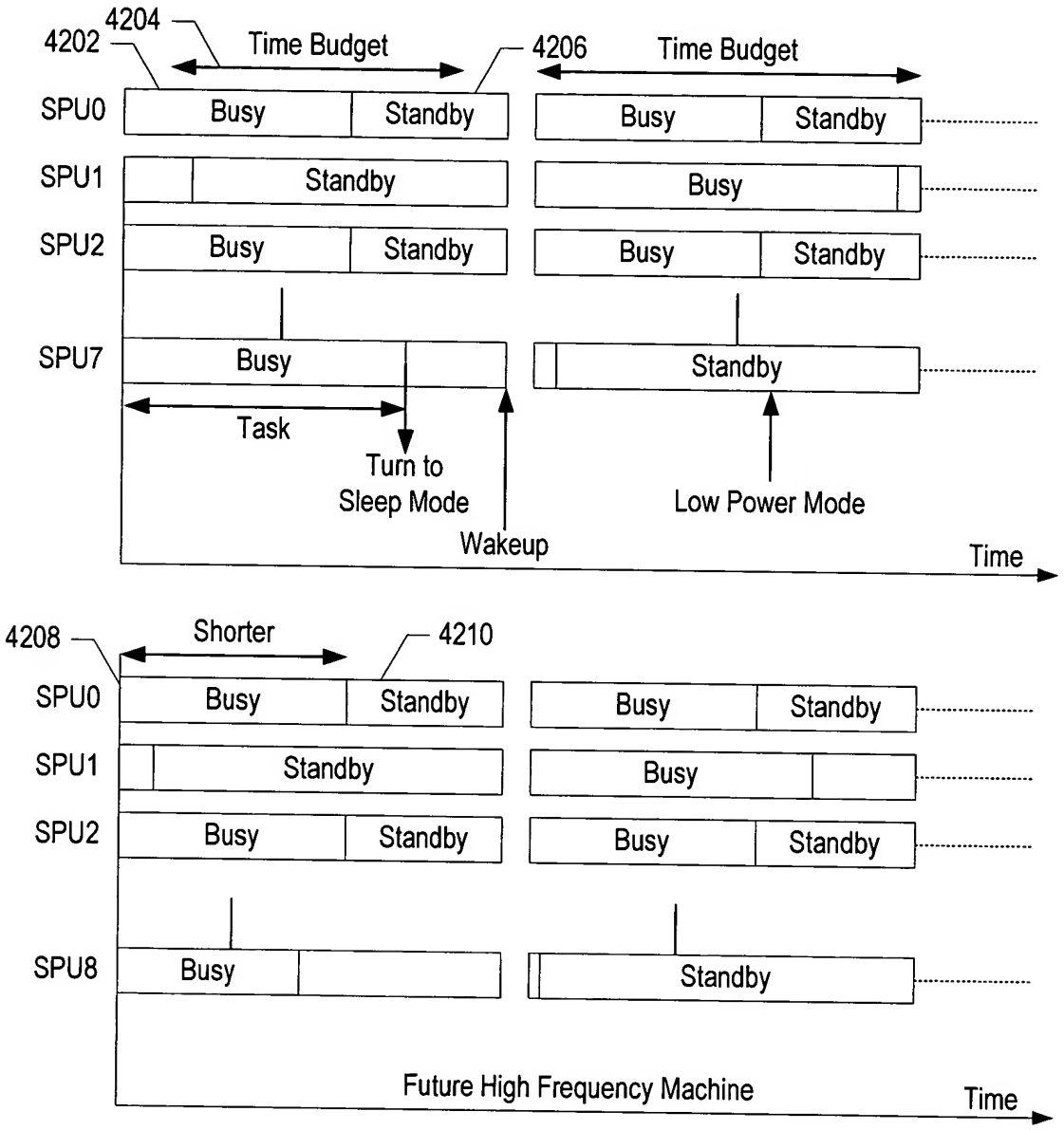
4202
4204
Time Budget
4206
Time Budget
SPU0
Busy
Standby
Busy
Standby
SPU1
Standby
Busy
SPU2
Busy
Standby
Busy
Standby
SPU7
Busy
Standby
Task
Turn to
Sleep Mode
Low Power Mode
Wakeup
Time
4208
Shorter
4210
SPU0
Busy
Standby
Busy
Standby
SPU1
Standby
Busy
SPU2
Busy
Standby
Busy
Standby
SPU8
Busy
Standby
Future High Frequency Machine
Time

Figure 42

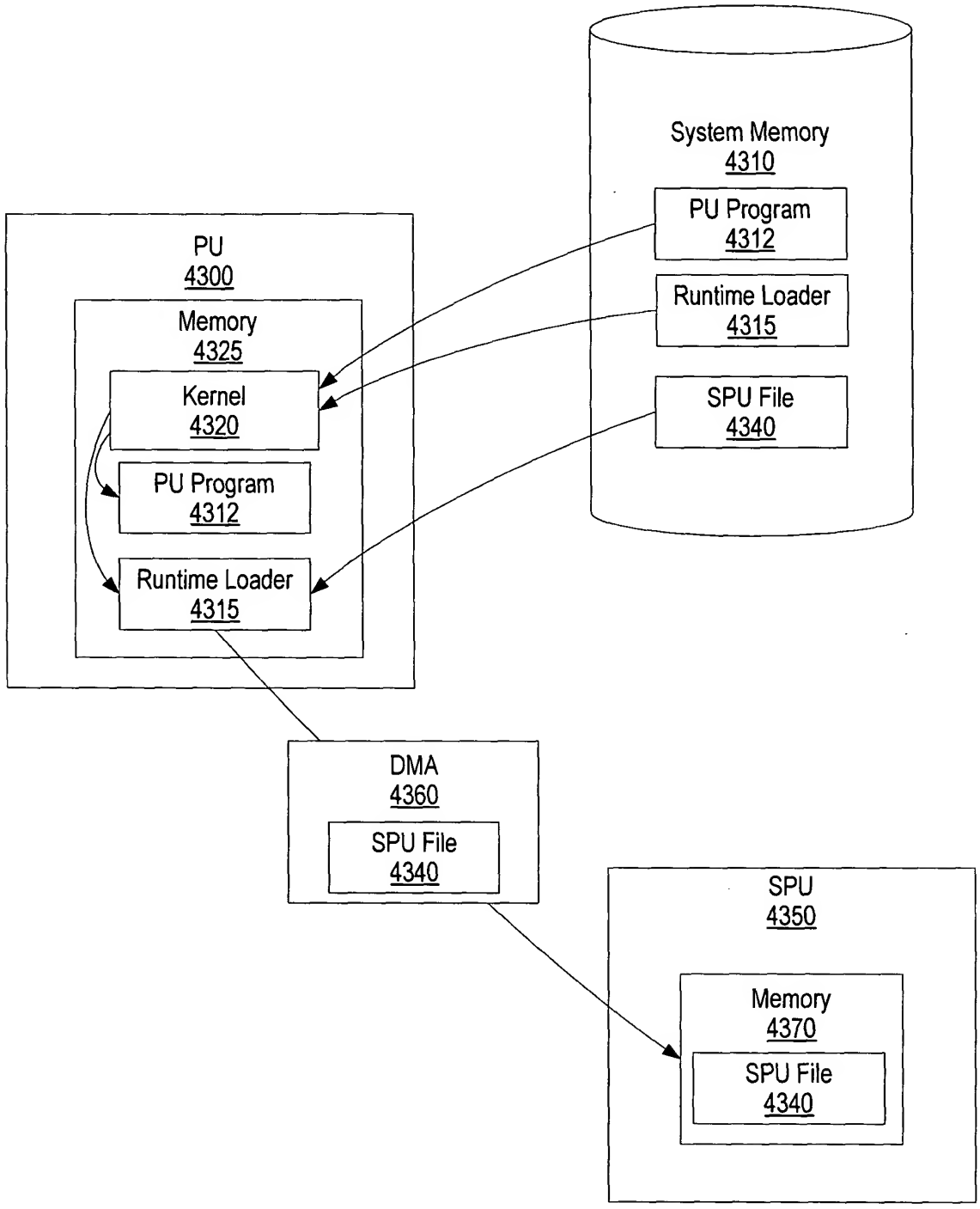
System Memory
4310
PU Program
4312
Runtime Loader
4315
SPU File
4340
PU
4300
Memory
4325
Kernel
4320
PU Program
4312
Runtime Loader
4315
DMA
4360
SPU File
4340
SPU
4350
Memory
4370
SPU File
4340

Figure 43

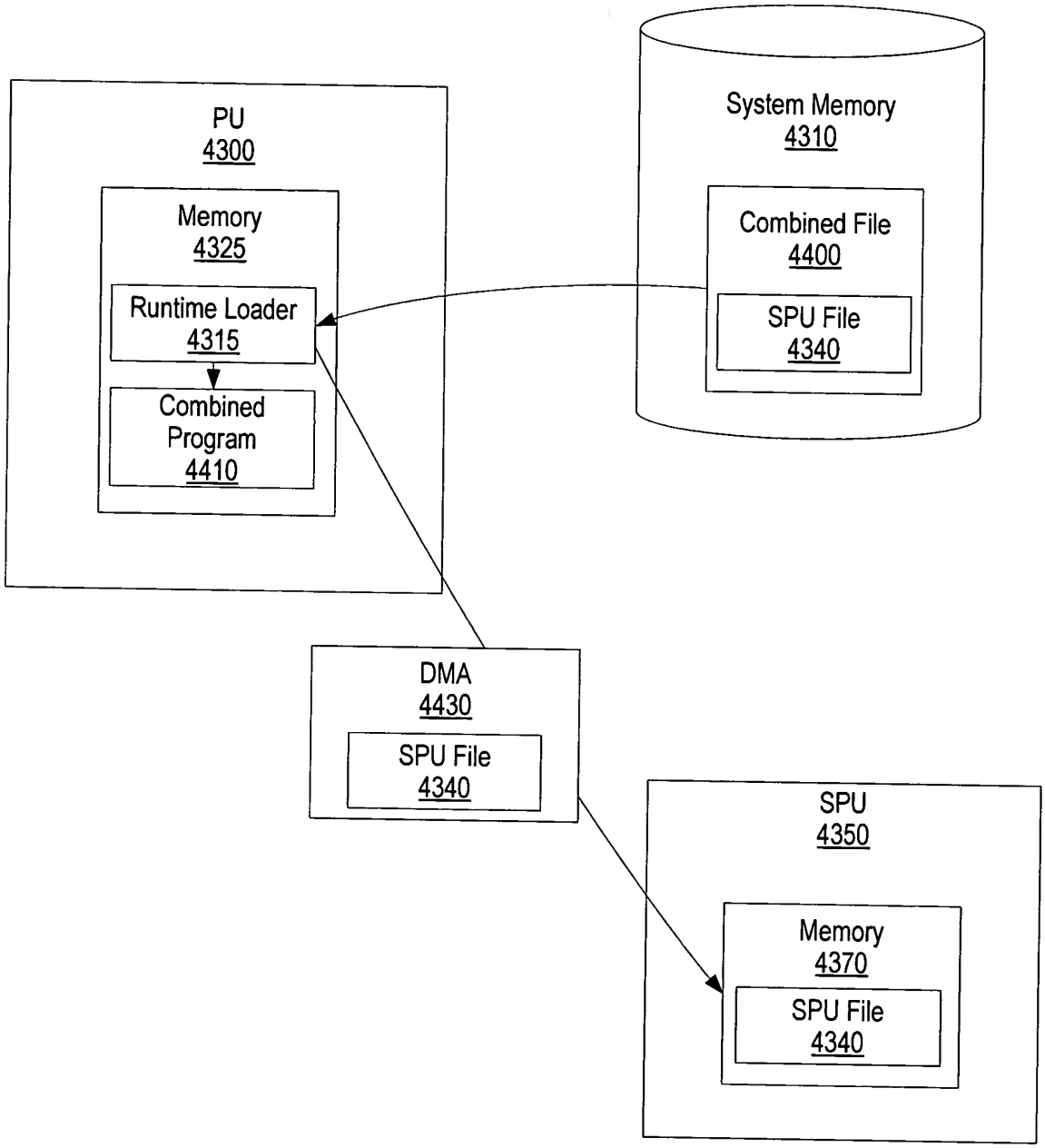
PU
4300
Memory
4325
Runtime Loader
4315
Combined
Program
4410
System Memory
4310
Combined File
4400
SPU File
4340
DMA
4430
SPU File
4340
SPU
4350
Memory
4370
SPU File
4340

Figure 44

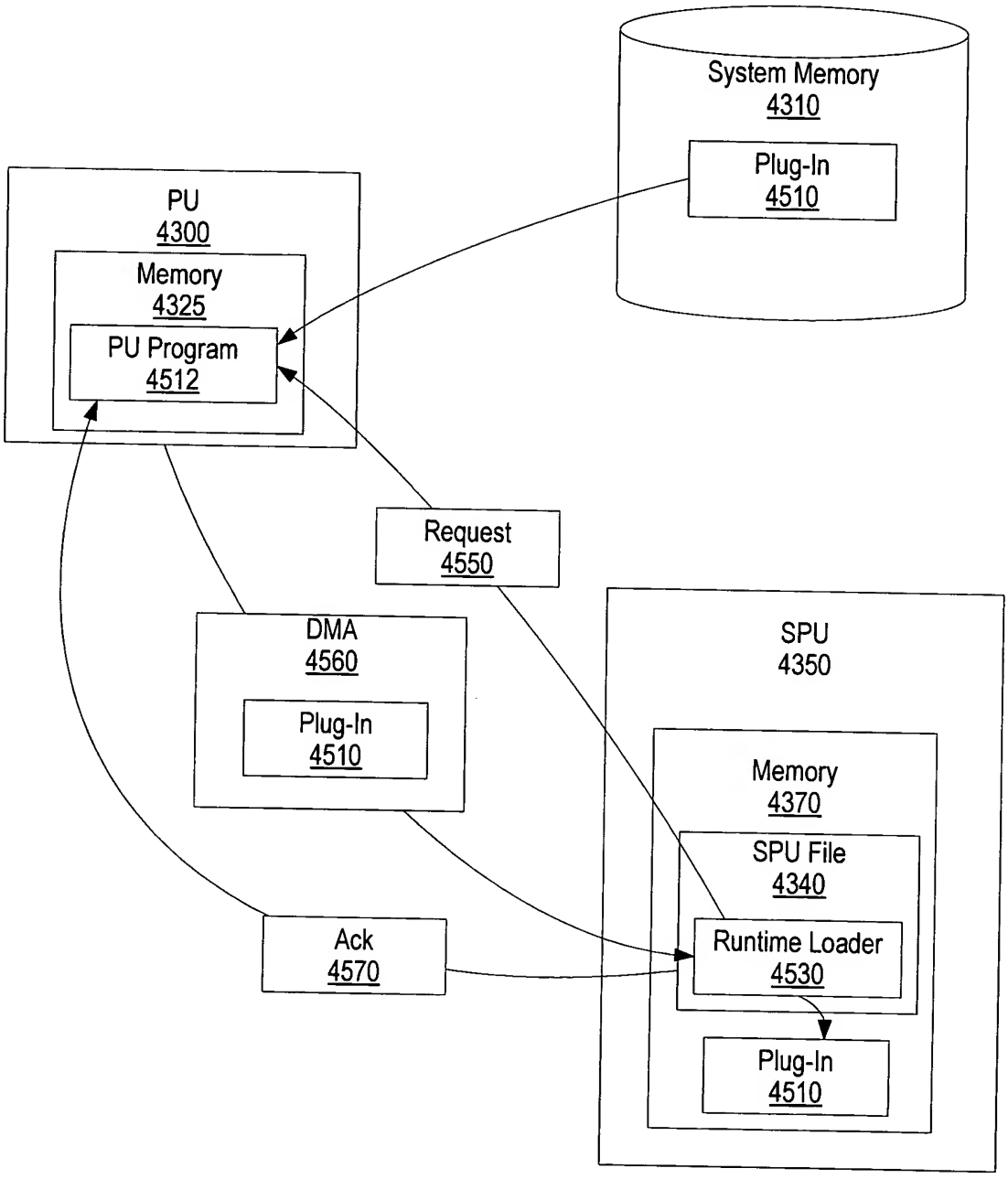
System Memory
4310
Plug-In
4510
PU
4300
Memory
4325
PU Program
4512
Request
4550
DMA
4560
Plug-In
4510
SPU
4350
Memory
4370
SPU File
4340
Runtime Loader
4530
Plug-In
4510
Ack
4570

Figure 45

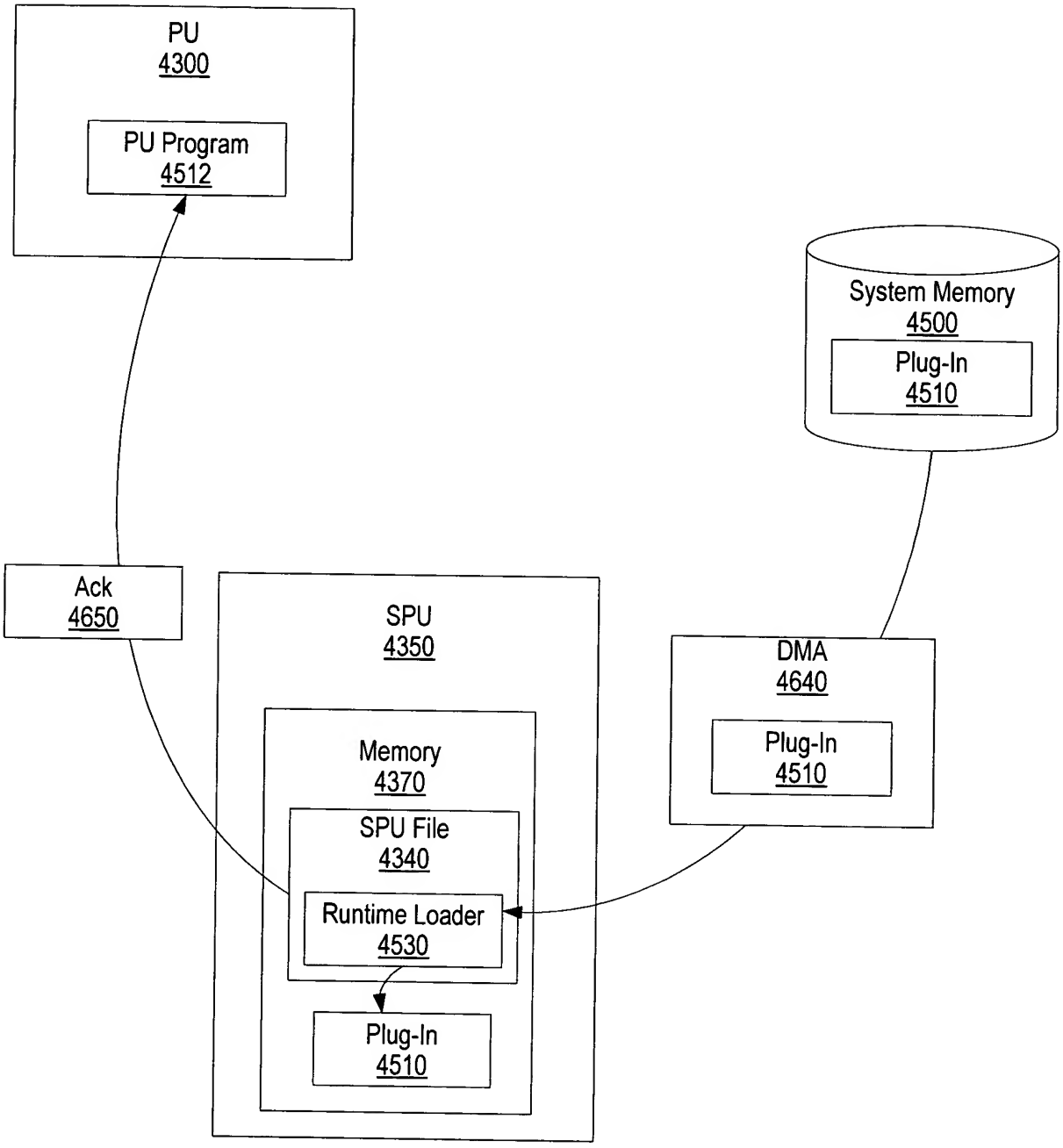
PU
4300
PU Program
4512
System Memory
4500
Plug-In
4510
Ack
4650
SPU
4350
DMA
4640
Memory
4370
Plug-In
4510
SPU File
4340
Runtime Loader
4530
Plug-In
4510

Figure 46

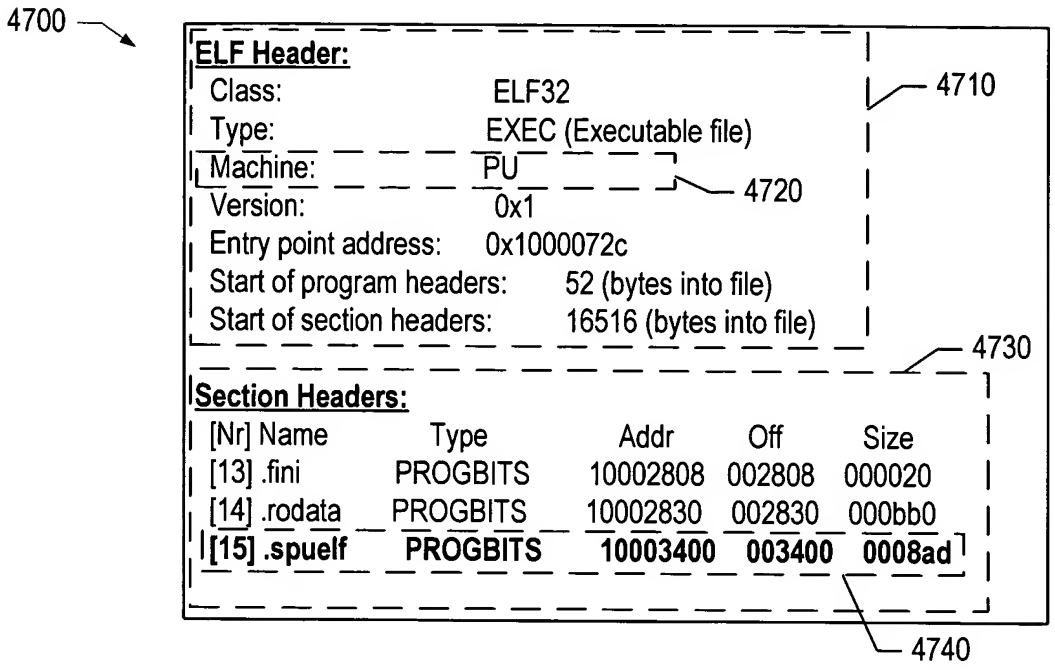

Figure 47A

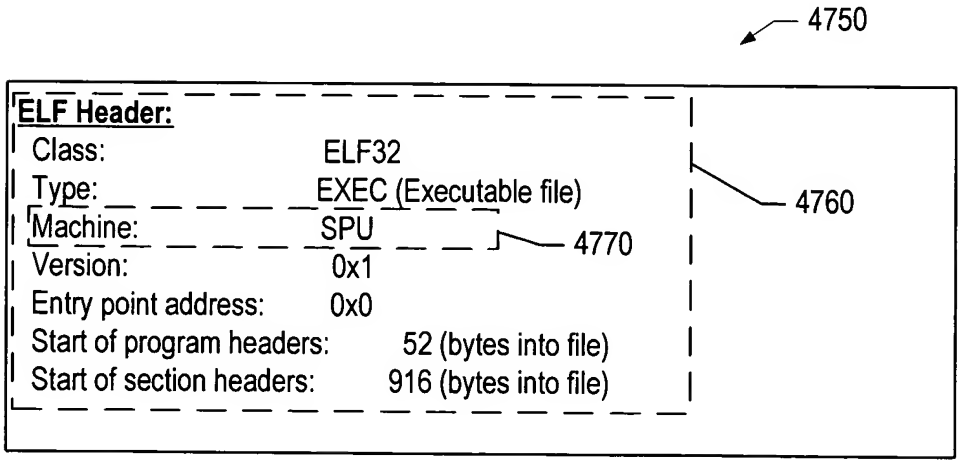

Figure 47B

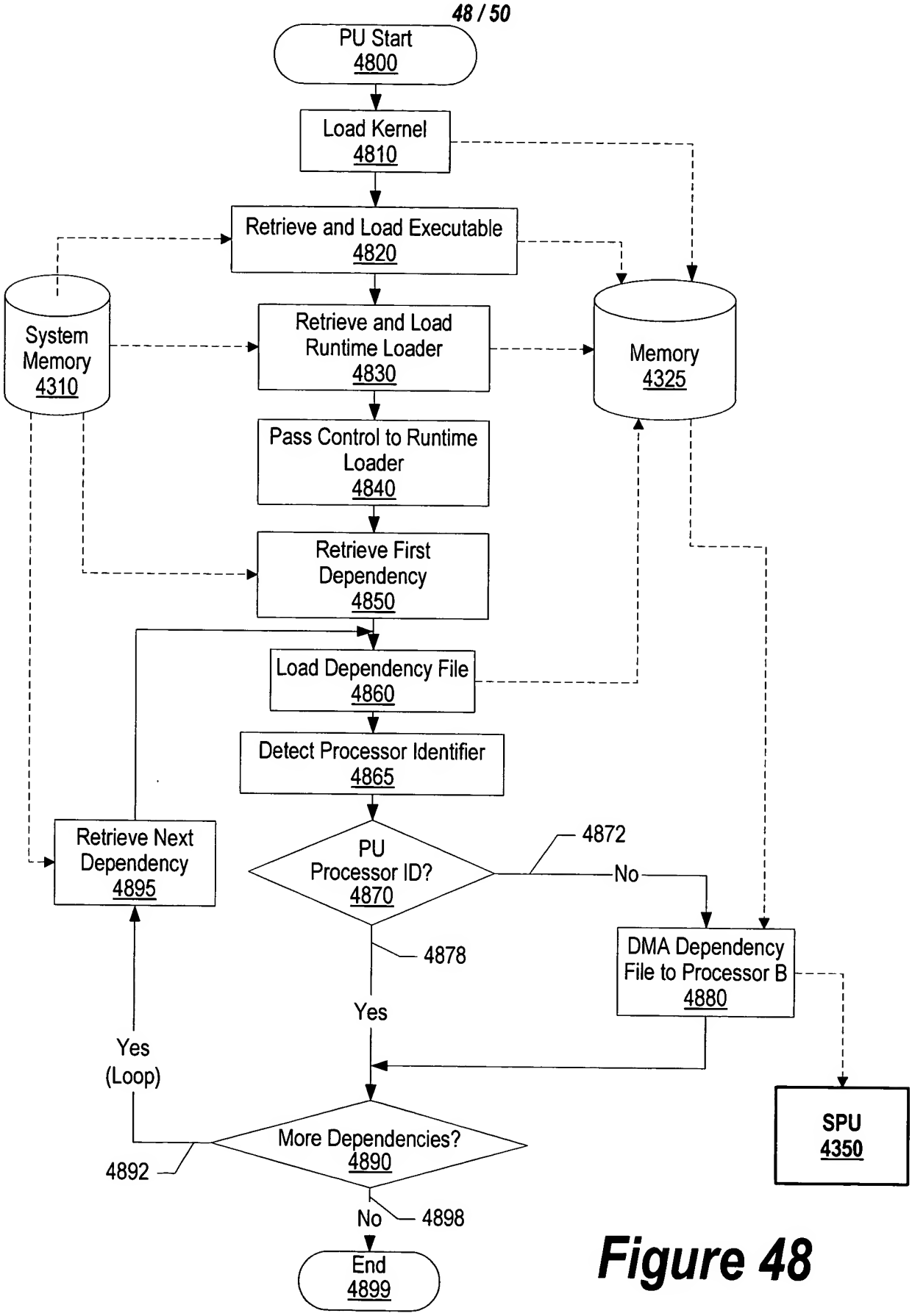
PU Start
4800
Load Kernel
4810
Retrieve and Load Executable
4820
System Memory
4310
Retrieve and Load Runtime Loader
4830
Memory
4325
Pass Control to Runtime Loader
4840
Retrieve First Dependency
4850
Load Dependency File
4860
Detect Processor Identifier
4865
Retrieve Next Dependency
4895
PU Processor ID?
4870
4872
No
4878
Yes
DMA Dependency File to Processor B
4880
Yes (Loop)
More Dependencies?
4890
4892
SPU
4350
No
4898
End
4899

Figure 48

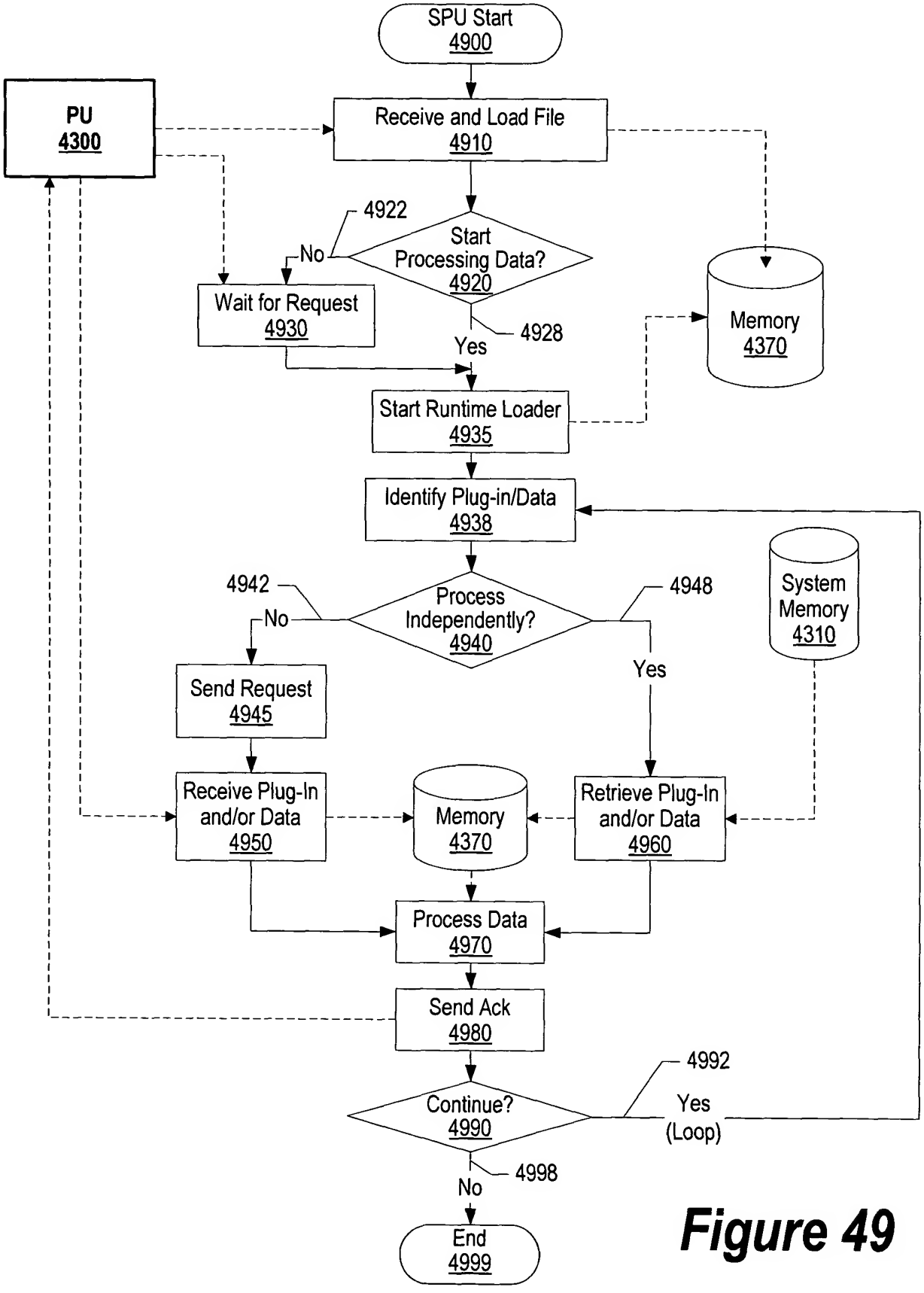
SPU Start
4900
PU
4300
Receive and Load File
4910
4922
Start
Processing Data?
4920
No
Wait for Request
4930
Yes
4928
Memory
4370
Start Runtime Loader
4935
Identify Plug-in/Data
4938
System
Memory
4310
4942
Process
Independently?
4940
4948
No
Yes
Send Request
4945
Receive Plug-In
and/or Data
4950
Memory
4370
Retrieve Plug-In
and/or Data
4960
Process Data
4970
Send Ack
4980
4992
Continue?
4990
Yes
(Loop)
4998
No
End
4999

Figure 49

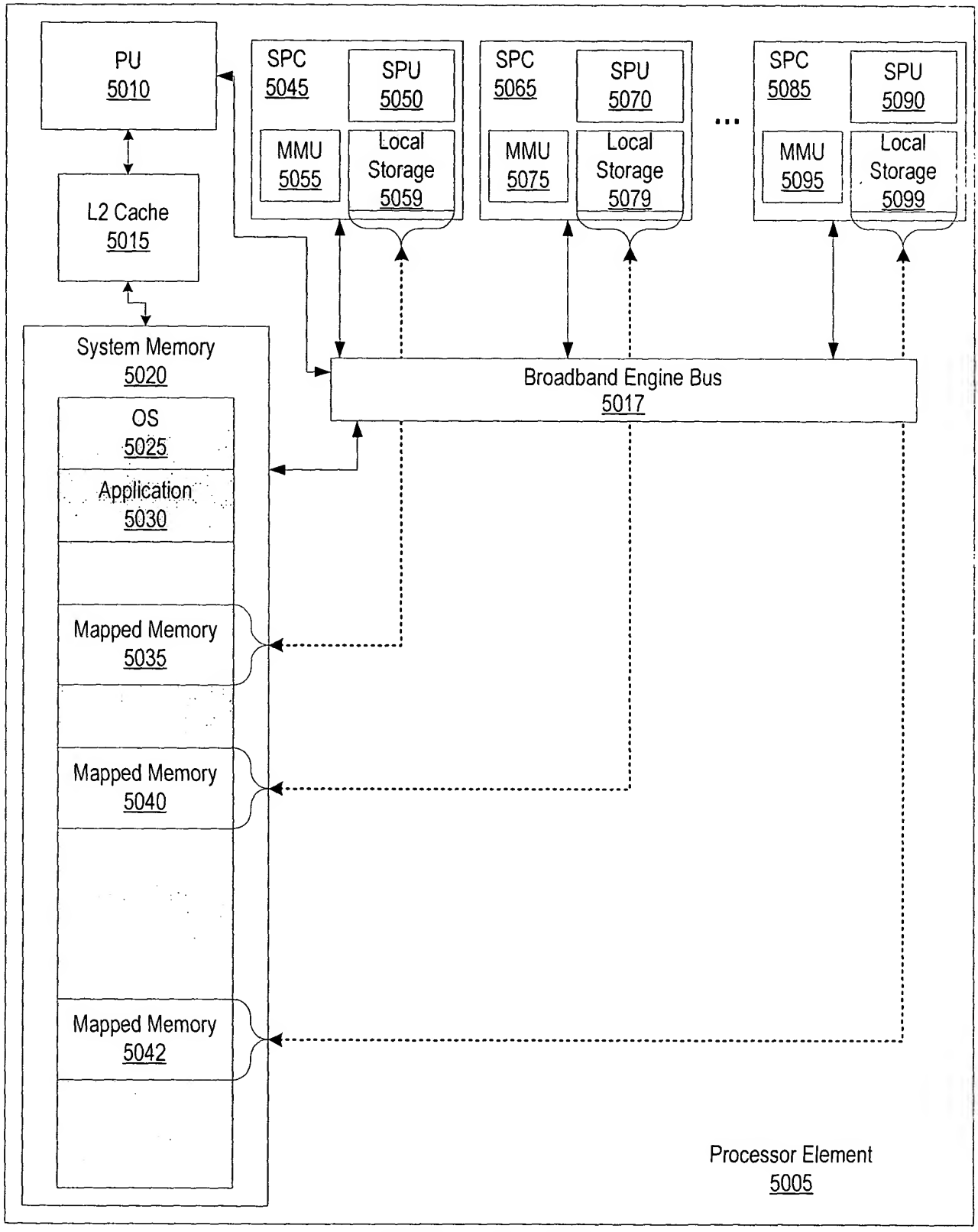
PU
5010
L2 Cache
5015
System Memory
5020
OS
5025
Application
5030
Mapped Memory
5035
Mapped Memory
5040
Mapped Memory
5042
SPC
5045
SPU
5050
MMU
5055
Local Storage
5059
SPC
5065
SPU
5070
MMU
5075
Local Storage
5079
...
SPC
5085
SPU
5090
MMU
5095
Local Storage
5099
Broadband Engine Bus
5017
Processor Element
5005

Figure 50